(1) 検出器
PADサイズ：1mm x 1mm (2mm x 2mm)
入力電荷量：電子数で100個から100,000個
シグナル立ち上がり：230-460nsec (グリッドとアノード間=0.5(1)mm)
drift time　0 - 110usec

(2) Preamp gain
　gain　6mV/fC 程度
　rise time　100nsec 程度
　decay time　1 - 10us (Preamp mode)

(3) Shaper
　gain　5 - 20倍（ ADCの仕様による）
　peaking time　0.5us, 1us, できれば、5usecまでvariableだとよい
　Diffusionによる時間方向のばらつき=σで460ns (24cmドリフト)

(4) ADC
　　10MHz程度, 10bit(少なくとも)
　　パイプライン読み出し

◆ **真空内外電気接続部品**

1) 超高真空対応カプトン絶縁被覆電線

同軸線　UHV対応

型　式	芯の本数	芯の直径[mm]	全体直径[mm]	導体面積[mm^2]	最大電圧[a] [kV DC]	最大電流[b] [A]	標準長さ [m]
311AC-KAP50S-1m [c) d)]	7	0.08	1.4	0.04	5	0.5	1
311AC-KAP50S [c) d)]	7	0.08	1.4	0.04	5	0.5	5
311AC-KAP50-1 [c)]	7	0.15	2.3	0.12	5	1	1
311AC-KAP50 [c)]	7	0.15	2.3	0.12	5	1	5
311AC-KAPM-060-COAX [e)]	19	0.1	1.4	0.15	1	2.5	10
311AC-KAPM-025-SHIELD [f)]	7	0.08	0.9	0.04	1	0.5	10

＜備考＞

a）値は真空内における最大電圧です。大気中の使用は避けてください。

b）真空内における最大電流値です。ただし、コイルの場合発熱問題があるため、最大電流を上記値の1/3
まで下げることを推奨します。

c）インピーダンス50Ω接続に対応します。

d）銀メッキ銅より線（311AC-KAPM-025）にシールドと絶縁被覆が付いたタイプです。

e）銀メッキ銅より線（311AC-KAPM-060）にシールドと絶縁被覆が付いたタイプです。
インピーダンスマッチングはされていません。

f）銀メッキ銅より線（311AC-KAPM-025）にシールドが付いたタイプです。
シールドの絶縁被覆はありません。インピーダンスマッチングはされていません。

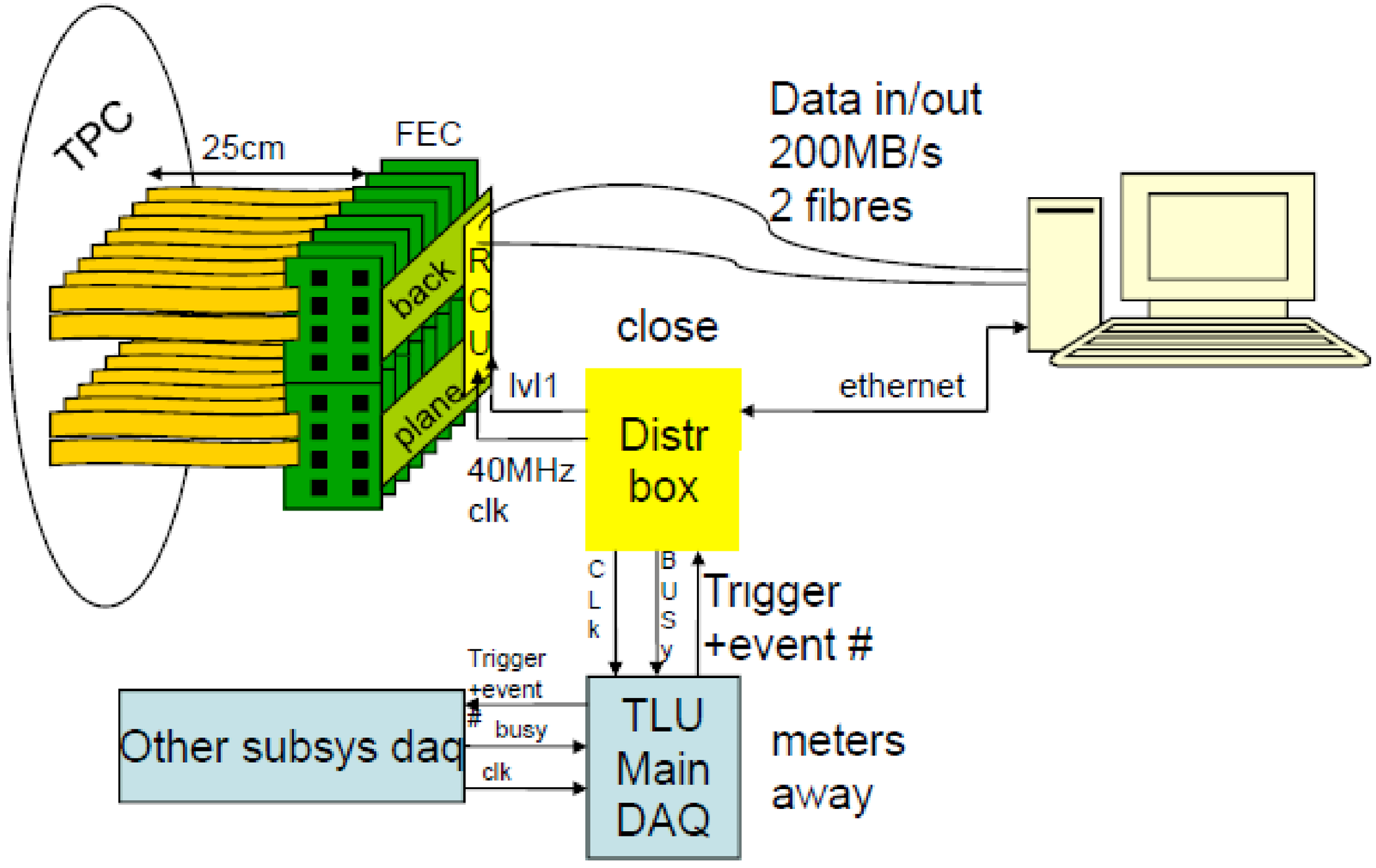
＜同軸カプトン線 311AC-KAPM-060-COAX＞

ドイツAllectra社の真空用カプトン®絶縁被覆電線

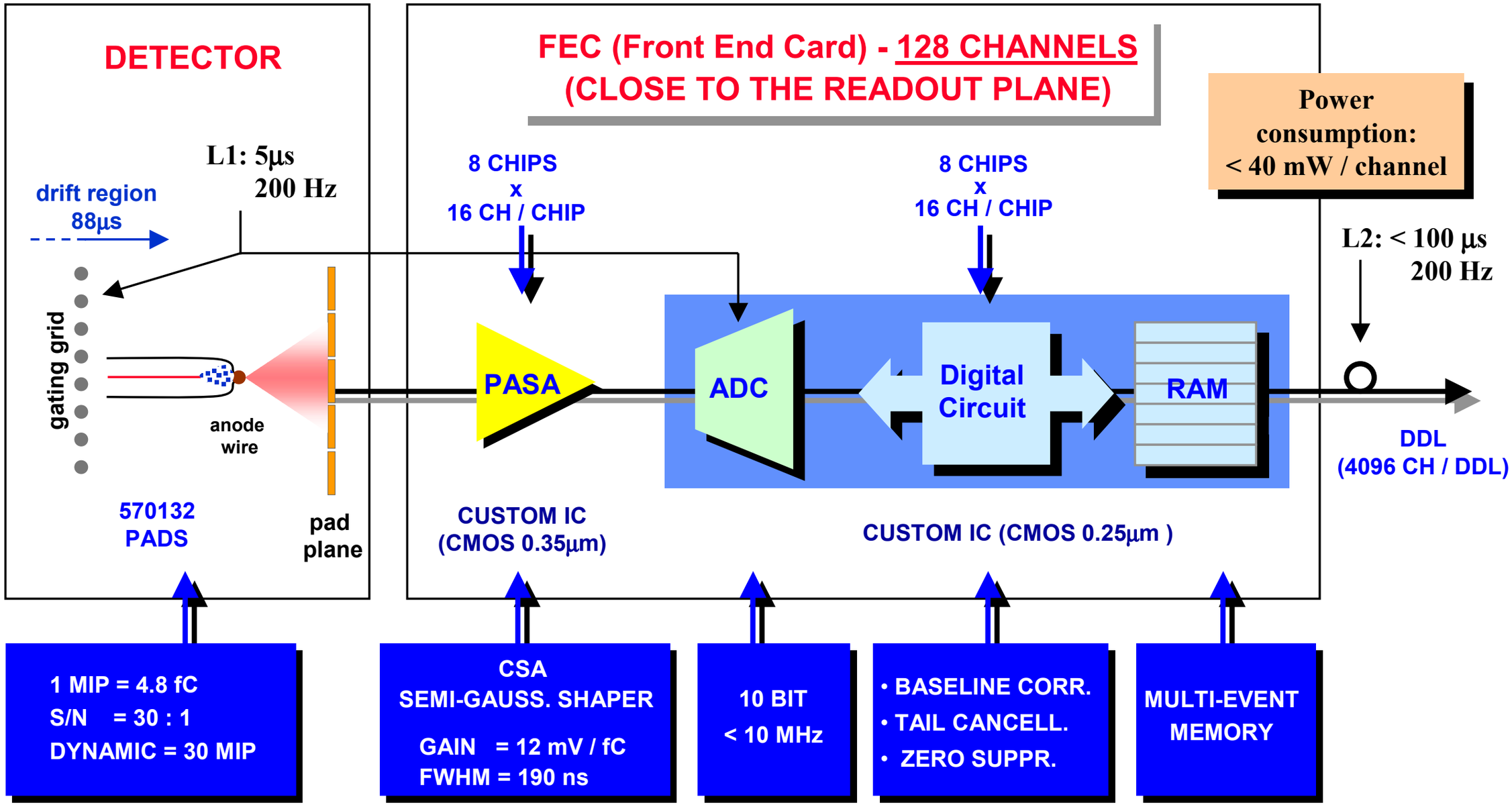
PMT	
signals	2+2
HV	2+2
TPC	
HV	1
Grid	1
signals	4+12
feedback	2+2?

ALTRO GEM Electronics

2048ch (16 FEC) (EUDET) → 10,000ch (LP test)



ARCHITECTURE



FEE for the NA49 and STAR TPCs:

- ◆ analog memory in front of the ADC ⇒ readout time independent of the occupancy
- ◆ no zero suppression in the FEE ⇒ high data throughput on the detector data links

PCA16 - modes of operation

Shaper Mode

3rd Order semi Gaussian Shaper (32 different configurations)				
Polarity	Positive (MWPC-like signals)		Negative (GEM-like signals)	
Conversion Gain (mv / fC)	12	15	19	27
Peaking Time (ns)	30	60	90	120

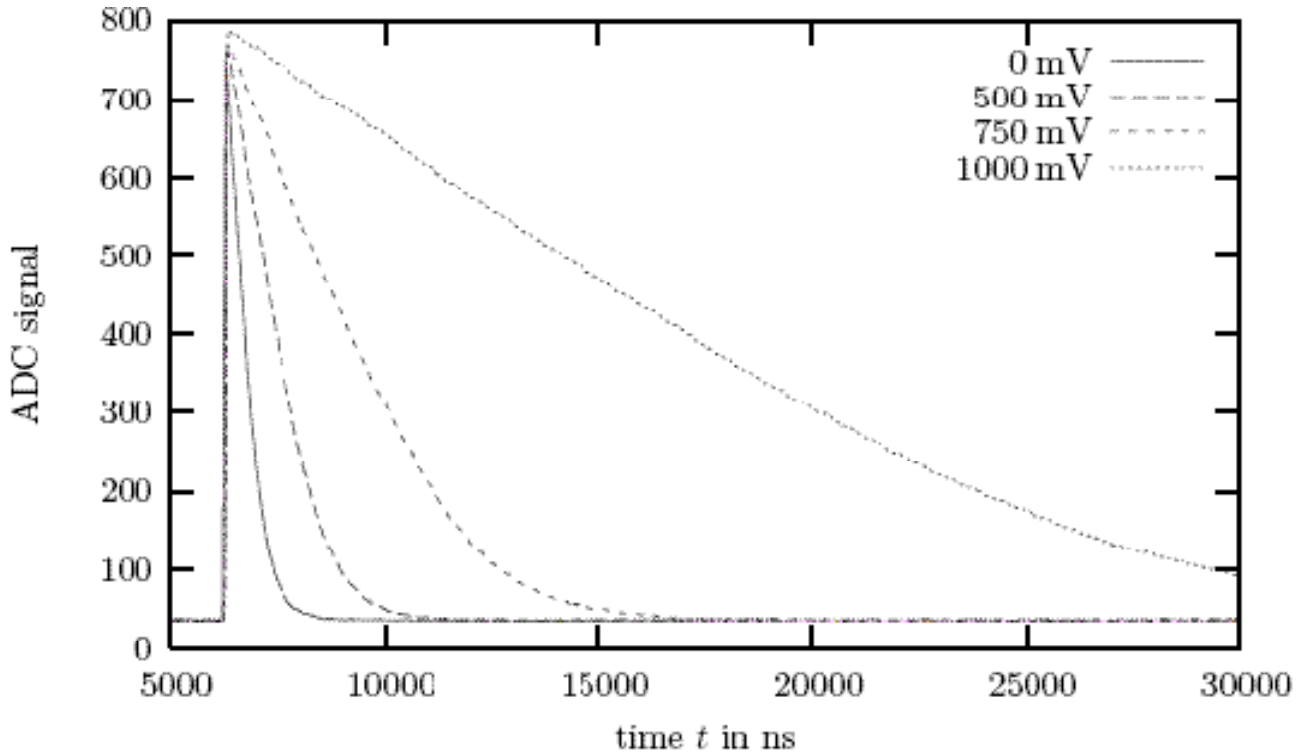
Preamp Mode

Classical CSA w/o PZ cancellation (32 different configurations)				
Polarity	Positive (MWPC-like signals)		Negative (GEM-like signals)	
Conversion Gain (mv / fC)	5.25	5.5	5.8	6.5
Rise Time (ns)	10	30	60	80
Decay Time (µs)	Continuous in the range [1:10]			

Performance very close to the design specifications in all modes of operation

Preamp Mode – Some Results

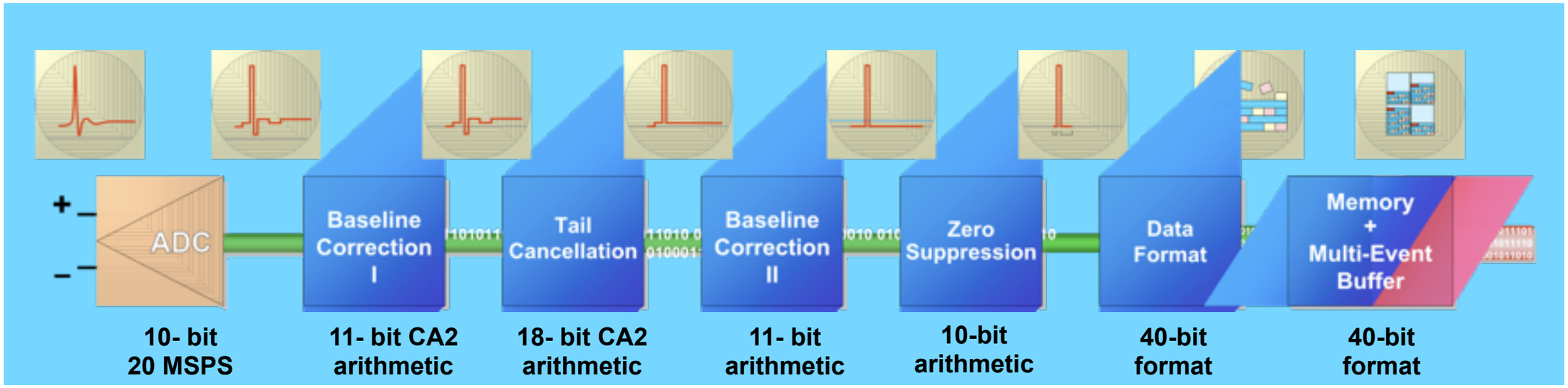
Negative Polarity (GEM-like Input Signal)



(b) different decay times

Figure 6: Impuls responce functions for selected combination of parameters.

ALICE TPC READOUT CHIP (ALTRO)

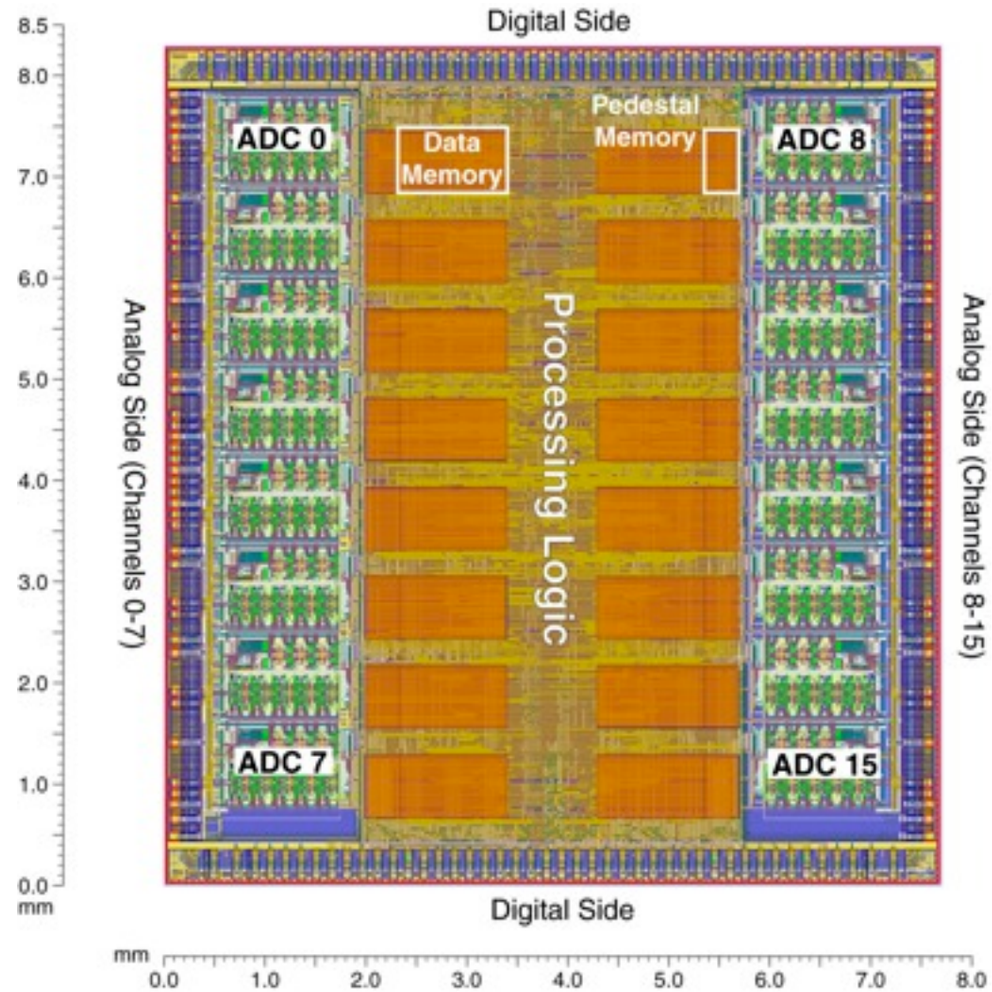


MAX SAMPLING CLOCK 40 MHz

MAX READOUT CLOCK 60 MHz

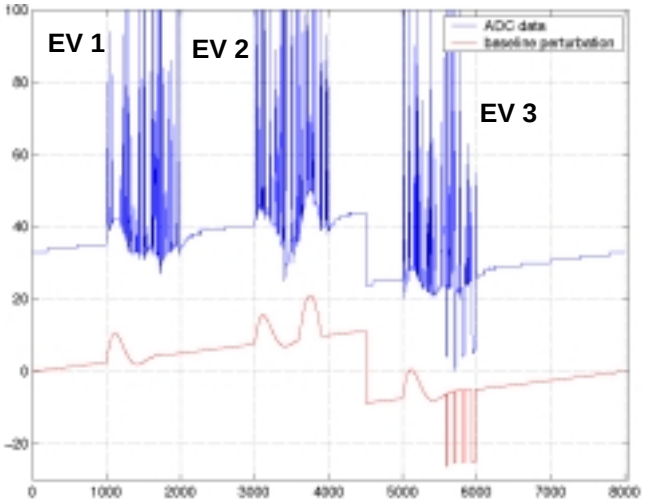
16-CH Signal Digitizer and Processor

- HCMOS7 0.25 mm (ST)
- area: 64 mm^2
- power: 16 mW / ch
- ADC ENOB: 9.5 (@ 10MHz)
- Data memory: 800 kbit
- output bandwidth: 300MB/s

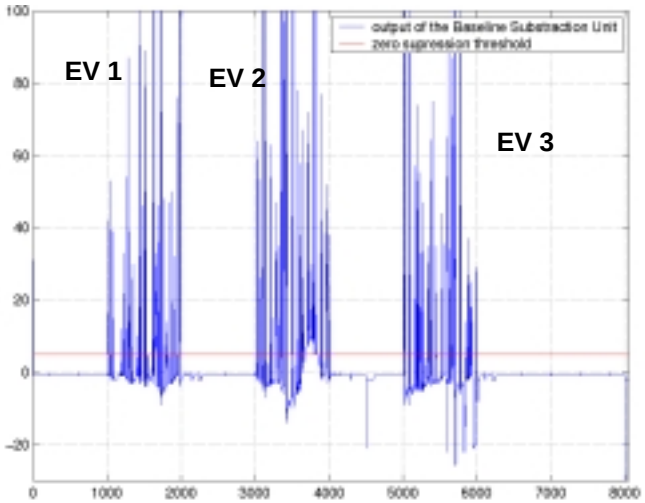


FRONT-END SIGNAL PROCESSING

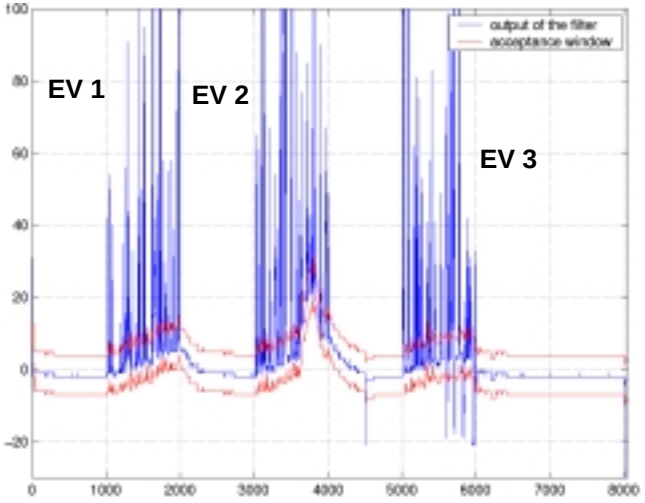
INPUT SIGNAL



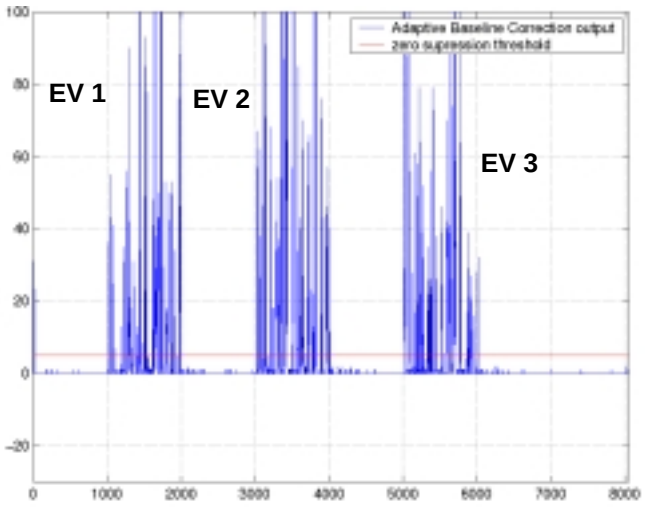
AFTER 1st BASELINE CORRECTION



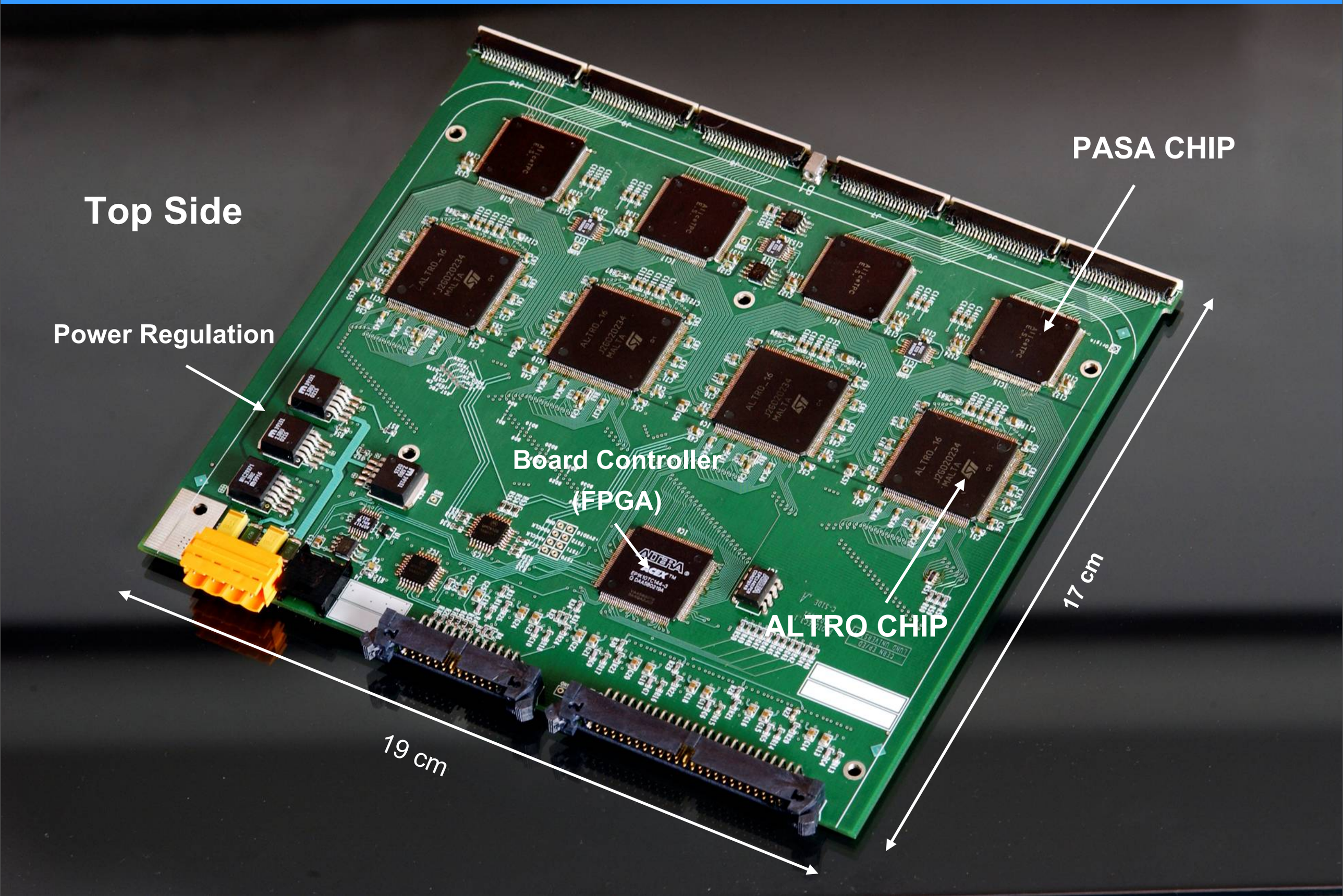
AFTER TAIL CANCELLATION



AFTER 2nd BASELINE CORRECTION



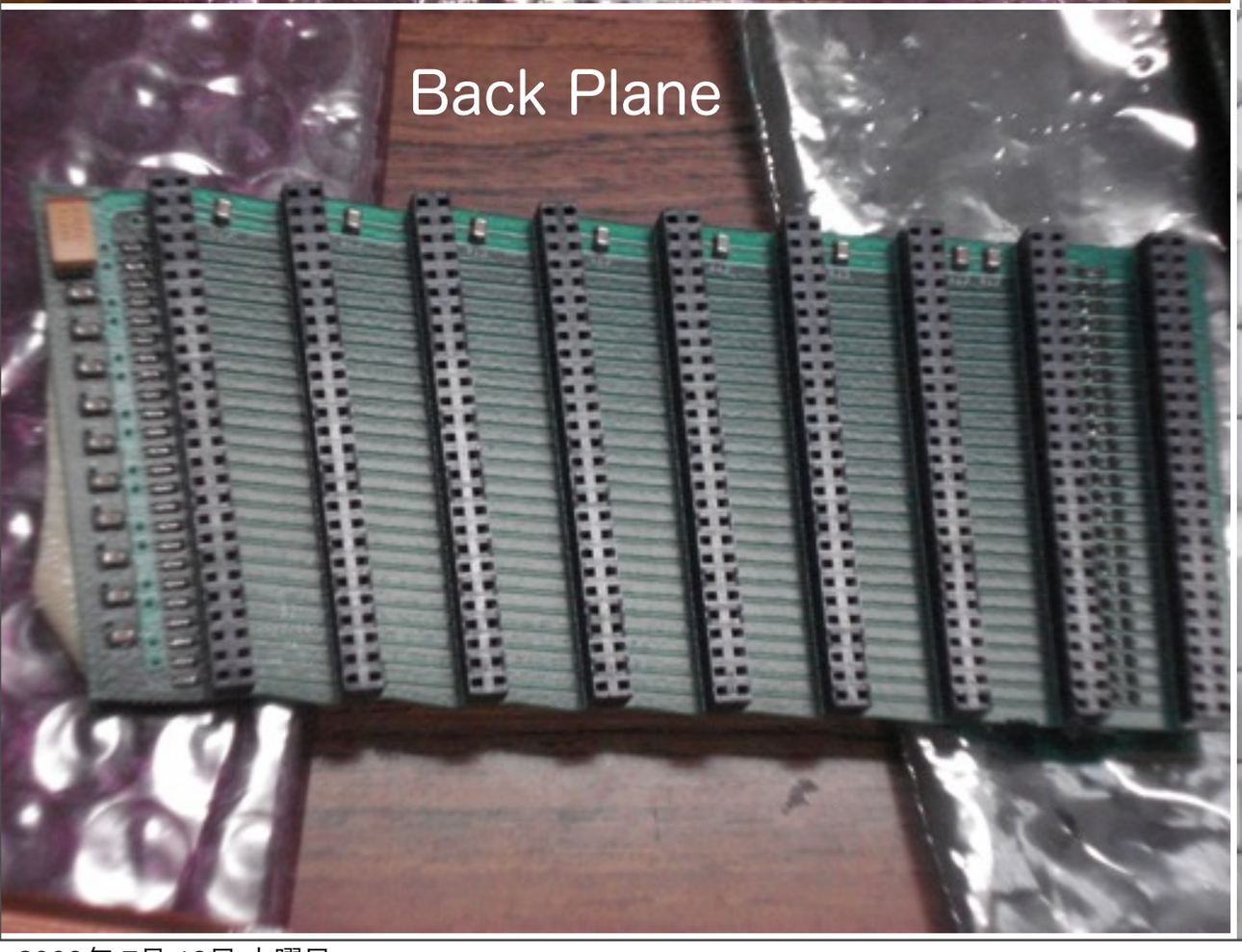
128-channel Front End Card



FEC (128ch)

RCU

Back Plane



Interface to PCI-X

AD[39:0] (bi-directional)

This is a 40-bit bi-directional Address/Data bus (table 2.2). It consists of three main fields that, starting from the least significant bit, are organised as follows: the *data* field (20 bits), the *instruction* field (5 bits) and the *address* field (14 bits). The most significant bit is a parity bit. It should be noted that, with a 14-bit *address* field, the ALTRO bus space sizes 16384. This addressable space is divided in two equal size partitions: the ALTRO chips partition (AL partition) and the Board Controller partition (BC partition).

39	38	37	36 29	28 25	24 20	19 0
PAR	ADDRESS				INSTRUCTION CODE	DATA
	BCAST	BC/AL	CHANNEL ADDRESS			

Table 2.2: 40-bit bi-directional Address/Data bus

AD[39] (PAR) is the parity bit of the 20 most significant bits. It is set such that the parity of the 20 most significant bits is always even. The parity bit allows the detection of a single bit error in the transmission between the RCU and the FEC.

When the bit AD[38] BCAST (broadcast) is set to 1, the *bus write cycle* initiated by the RCU (master) is addressed to an entire *partition* of the *address space* (AL or BC partition). In this case the slave units ignore the channel address field.

The bit AD[37] (BC/AL) defines the address space partition: 1 for the BC partition, 0 for the AL partition.

The following 12 bits AD[36:25] (CHANNEL ADDRESS) specify the *channel address* and, during an *instruction cycle*, are compared with the hard-wired address. From the most significant bit, the channel address consists of a branch address (1 bit), the FEC address (4 bits), the ALTRO chip address (3 bits) and the ALTRO's internal channel address (4 bits). This allocations of addresses is the recommended one and it corresponds to the case of a board containing 8 ALTROs (FEC) and an RCU with two branches each one with 16 FECs.

The bits AD[24-20] (INSTRUCTION CODE) carry the instruction code. As it will be detailed in the next section, the ALTRO chips and the BC are controlled by a set of instructions. The instruction can be either an access to a Configuration/Status Register (CSR), whose address is part of the instruction code, or a Command. In the former case, the instruction involves a WRITE or READ cycle, according to the value of the WRITE signal, to one of the CSRs. In the latter case the instruction does not imply a data transfer from/to the addressed unit, thus the data field of the AD bus is not used.

The data field AD[19-0] carries the data in the WRITE or READ instructions.

http://www.hep.lu.se/eudet/

20 bits DATA :
ADC 10bits
Time 10bits

2 x 16 FECs / RCU

8 ALTRO / FEC
16ch/ALTRO

12 bits address :
a branch address (1bit)
FEC address (4bits)
ALTRO chip address(3bits)
ALTRO's internal ch address(4bits)