# Laser Compton meeting

Jan. 27  H. Yoshitama

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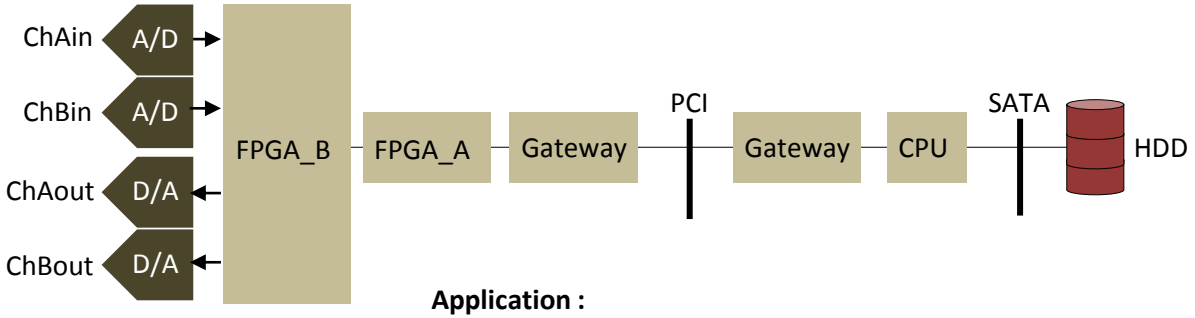
# Design status history

## Original 4DSP design




**Record :**
ADCAbuffer.bin
ADCBbuffer.bin

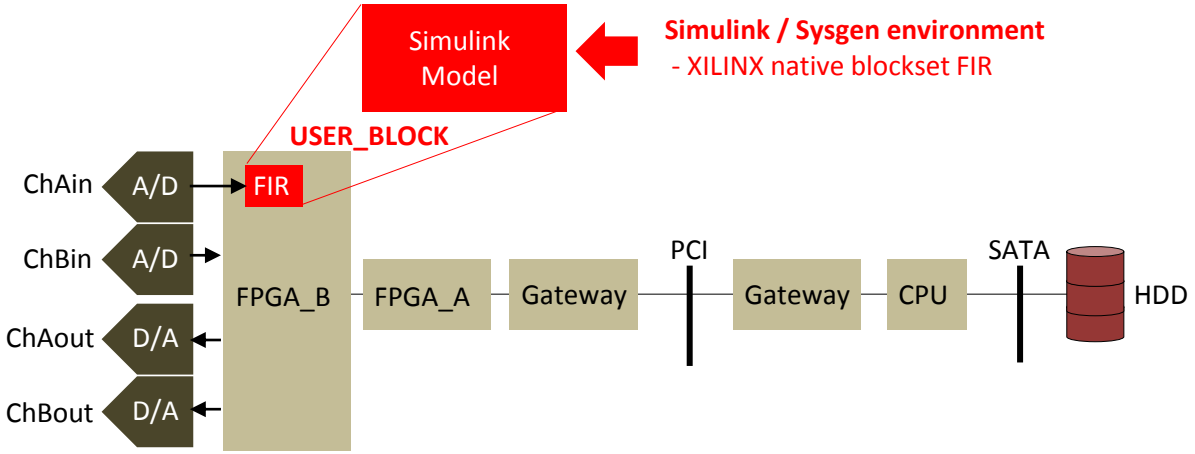
**Playback :**
dacawf.bin
dacbwf.bin

**Application :**

- Record : ChaAin and ChBin are stored in HDD (4095 bytes)
- Playback : Signals are generated on the outputs ChAout and ChBout

**PURPOSE : demonstrates the use of SYSGEN with FM485 board**

## MISH modification




**Record :**
ADCAbuffer.bin
ADCBbuffer.bin

**Playback :**
dacawf.bin
dacbwf.bin

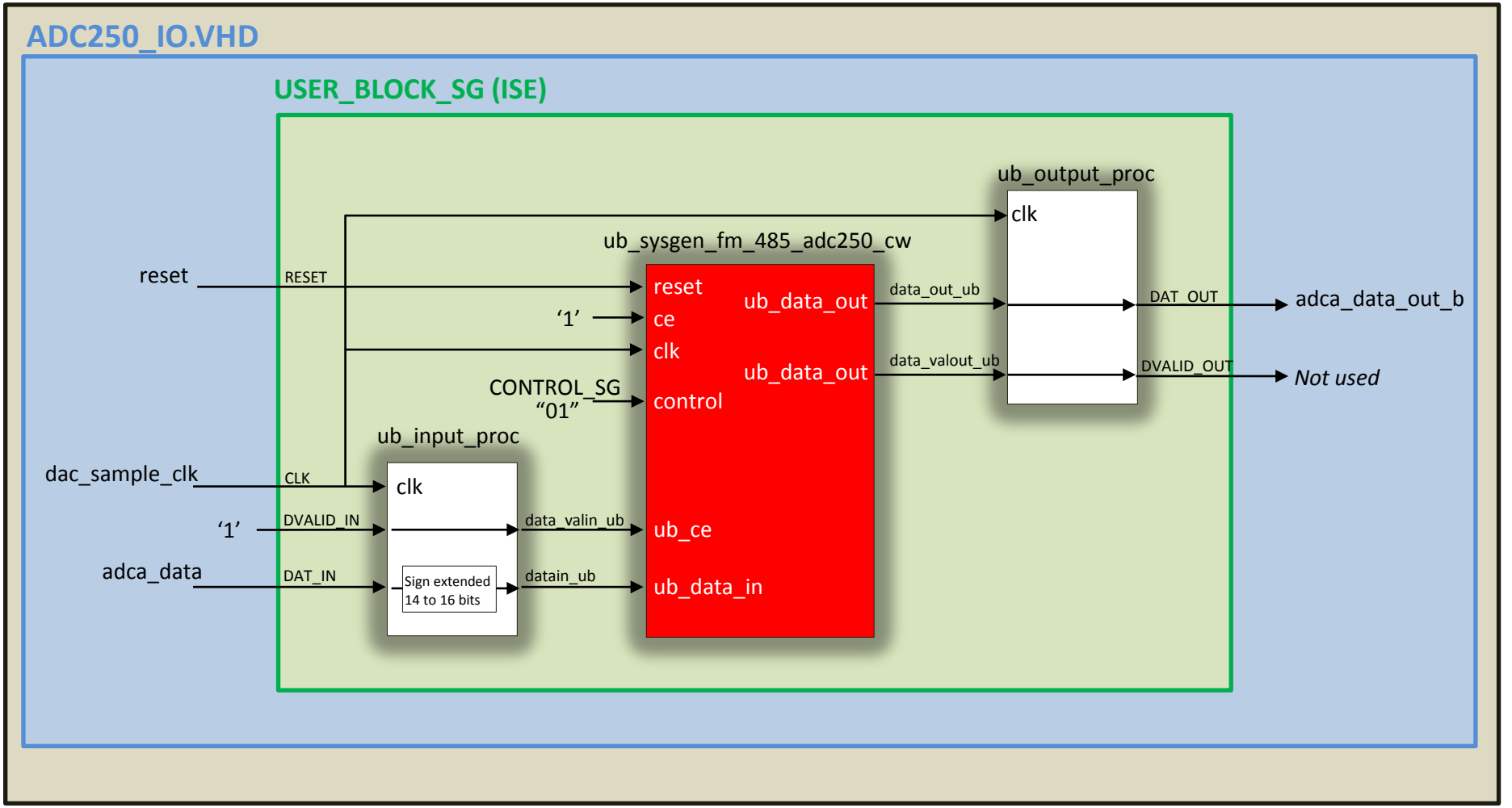
**Application :**

- Record : ChaAin with FIR and ChBin are stored in HDD (4kb)
- Playback : Signals are generated on the outputs ChAout and ChBout

# User_Block integration diagram

## FM485_FPGA_B

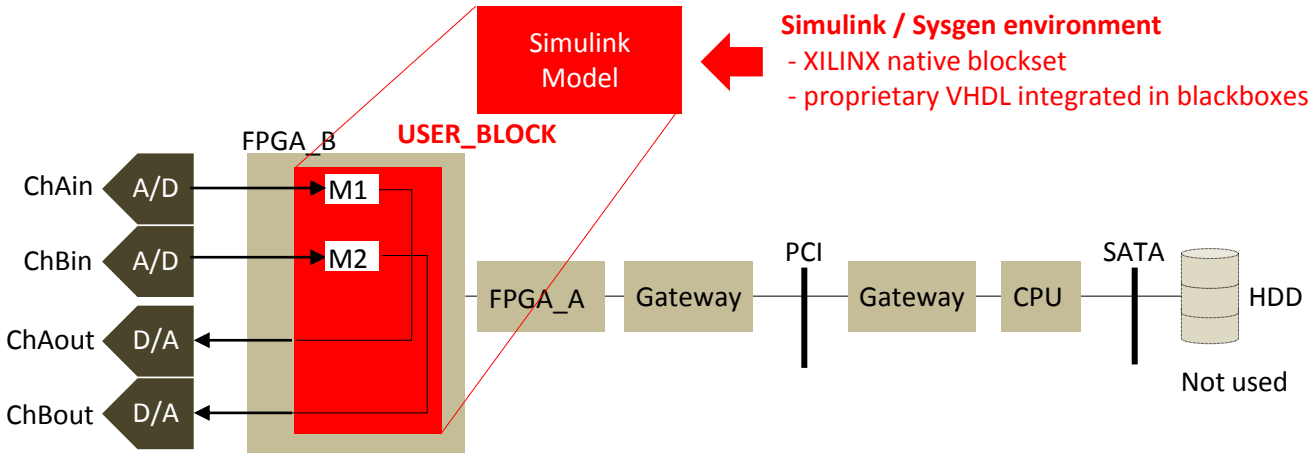
**This is how the USER_BLOCK is connected to FPGA_B**



# Present Design on 2012.01.27

**Hiroshima design on 20112/01/27**

**This week's work**



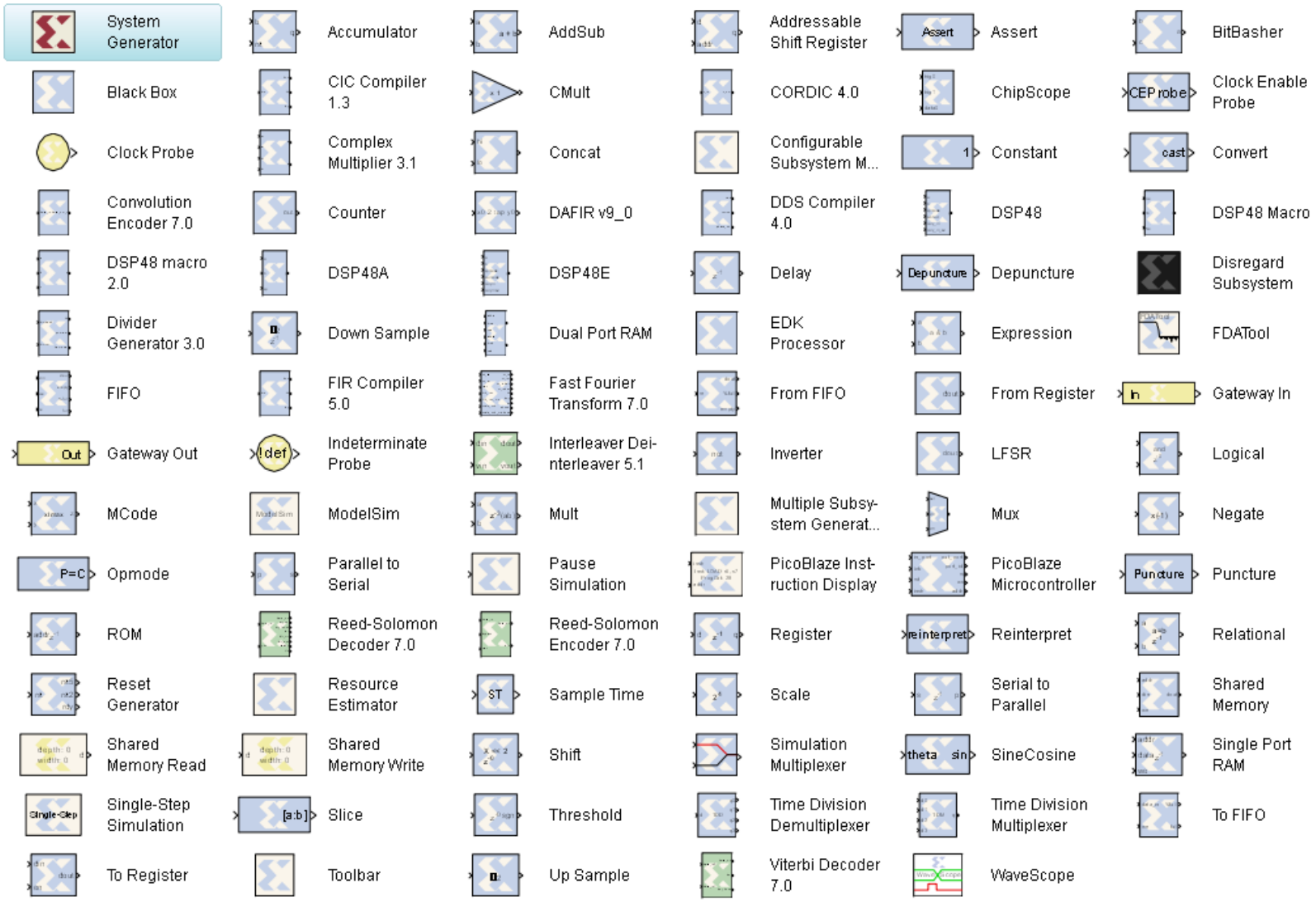

**Application :**

- Module M1 : Feedback regulation
- Module 2 : not yet defined

# MATLAB/Simulink blocksets

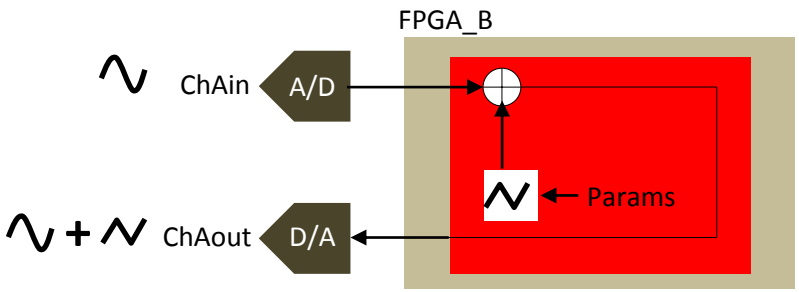
Simulink Model

**Simulink / Sysgen environment**
- XILINX native blockset
- proprietary VHDL integrated in blackboxes



# MATLAB/Simulink example

## Test example

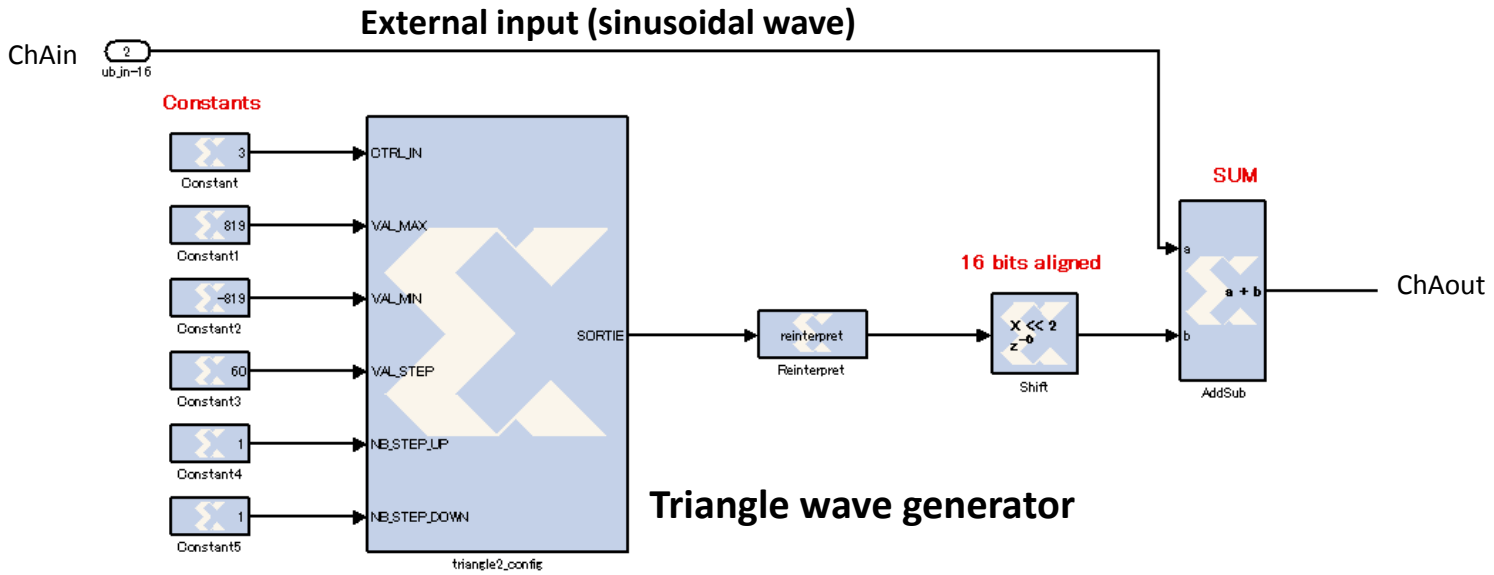



Black Box

1- I generate a triangle wave signal (VHDL block)
the parameters are used for frequency and amplitude

2- I sum the Ch A input with the triangle wave

## Design

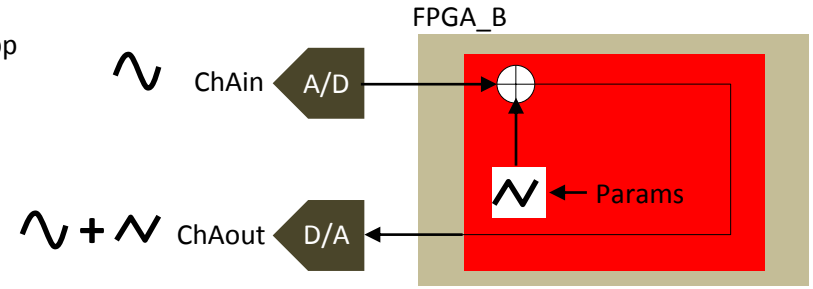



## Limitation

In this design, the parameters are **constants**. I can't modify them **dynamically**. I need to reconfigure the FPGA. **Conclusion**: not convenient for all designs (PID, A/D D/A gains, debug,…)

# MATLAB/Simulink example

**Amplitude** : 50mVpp
**Frequency** : 3MHz




**Triangle Parameters**

**Amplitude** : 100mVpp
**Frequency** : 350kHz

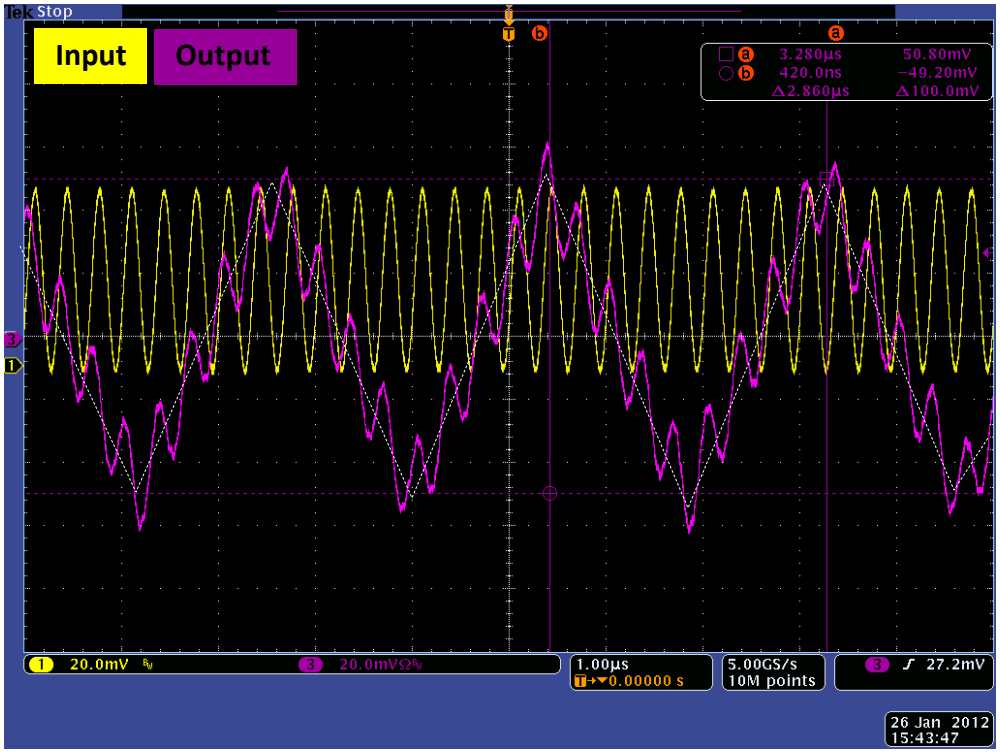
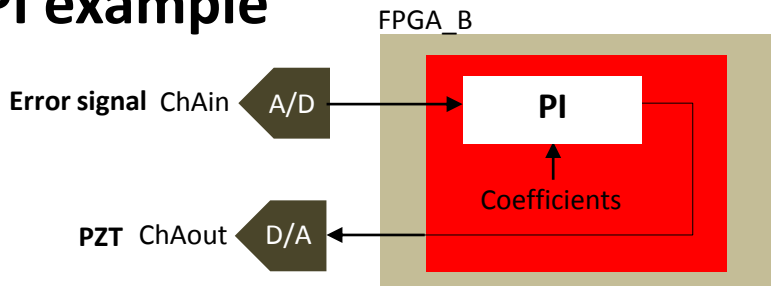



**Fig. 1** : Input signal (sine wave ) – Output signal

# MATLAB/Simulink example

## PI example




1- I use Xilinx native blocksets to implement a PI.
2- I use Simulink functionalities to simulate the design.

**Discrete input, output**

$e_k$: Input $u_k$: Output

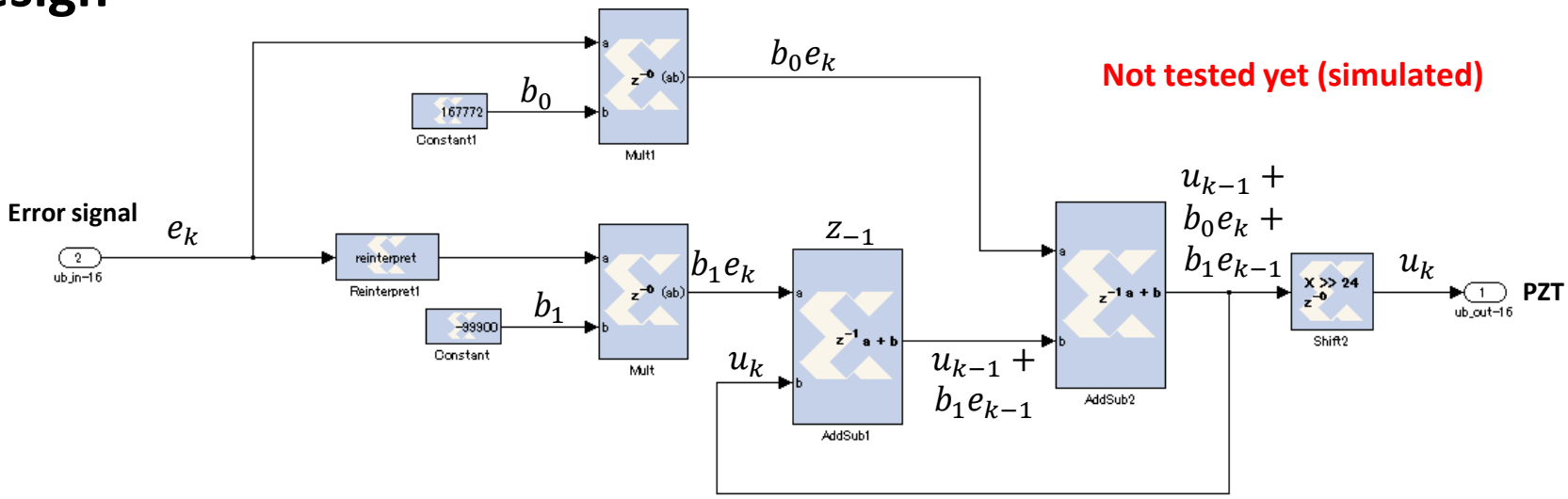
**PI discrete equation**

$$u_k = u_{k-1} + b_0 e_k + b_1 e_{k-1}$$

**Coefficients value = F(Kp,Ti,Ts)**

$$b_0 = K_P \qquad b_1 = K_P\left(-1 + \frac{T_s}{T_I}\right)$$

## Design



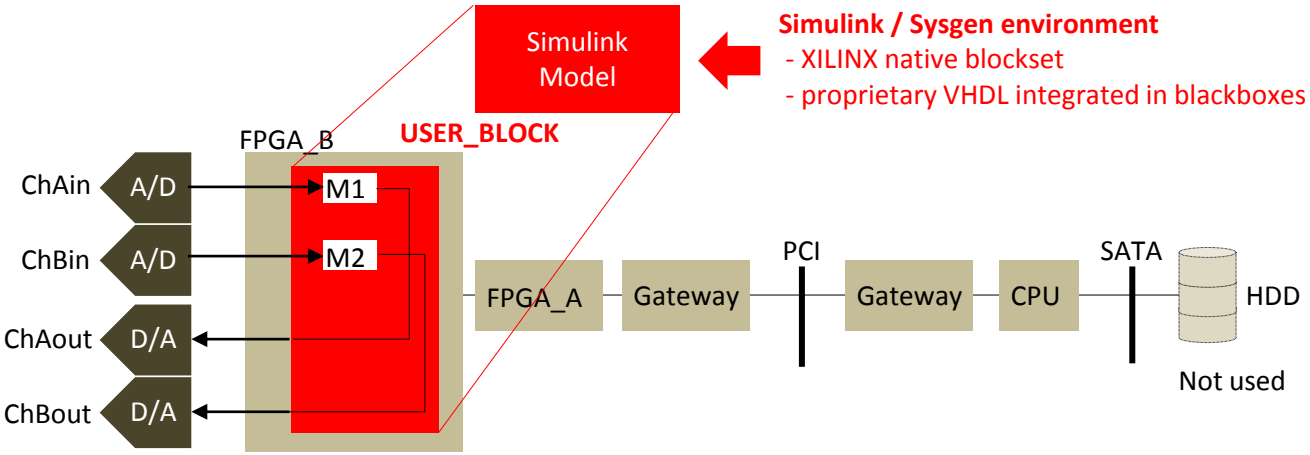

## Limitation

In this design, the PI coefficients are **constants**. I can't modify them **dynamically**. I need to reconfigure the FPGA. **Conclusion** : not convenient for our feedback design.

# Design requirement

## Feedback need (1)

**This is what we have on 20112/01/27**



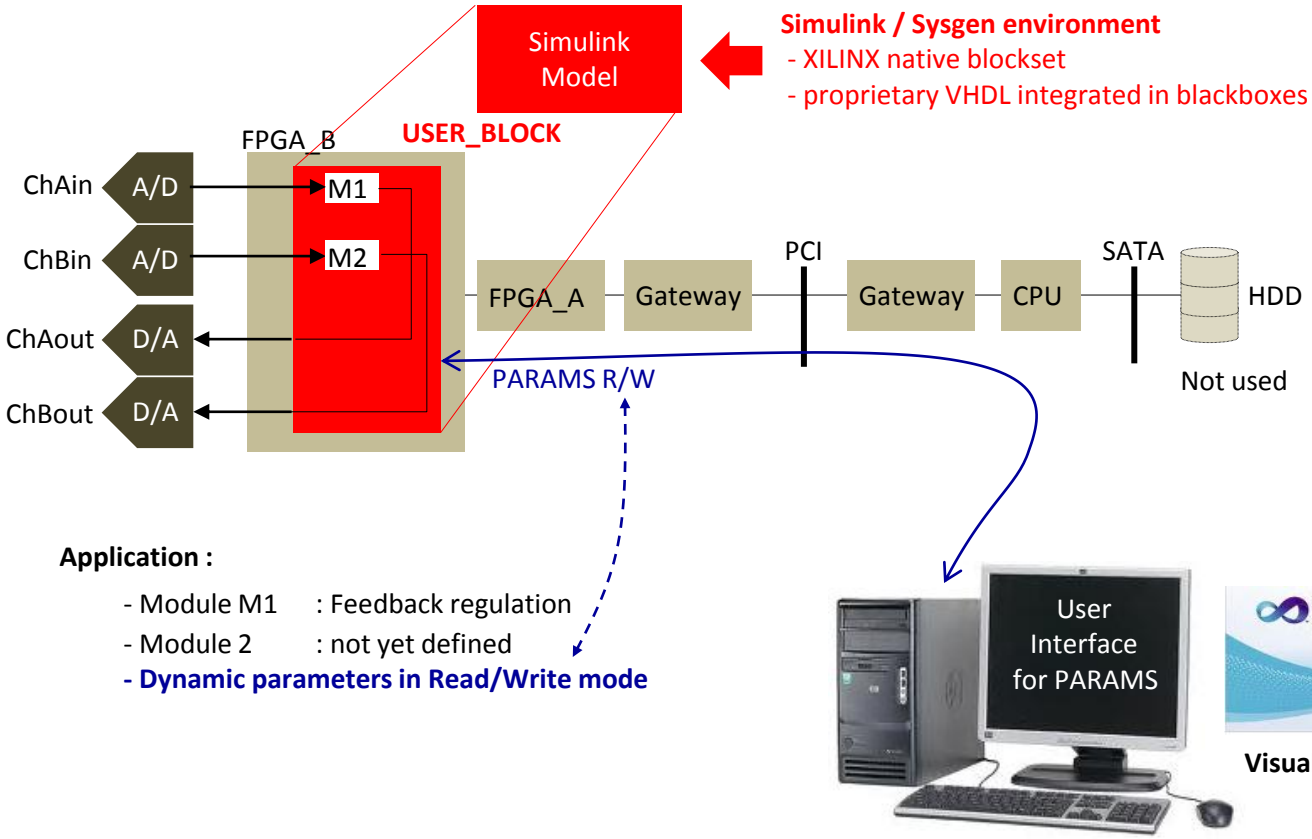

**Application :**

- Module M1 : Feedback regulation
- Module 2 : not yet defined

# Design requirement

## Feedback need (2)

**This is what we want on 20112/01/27**



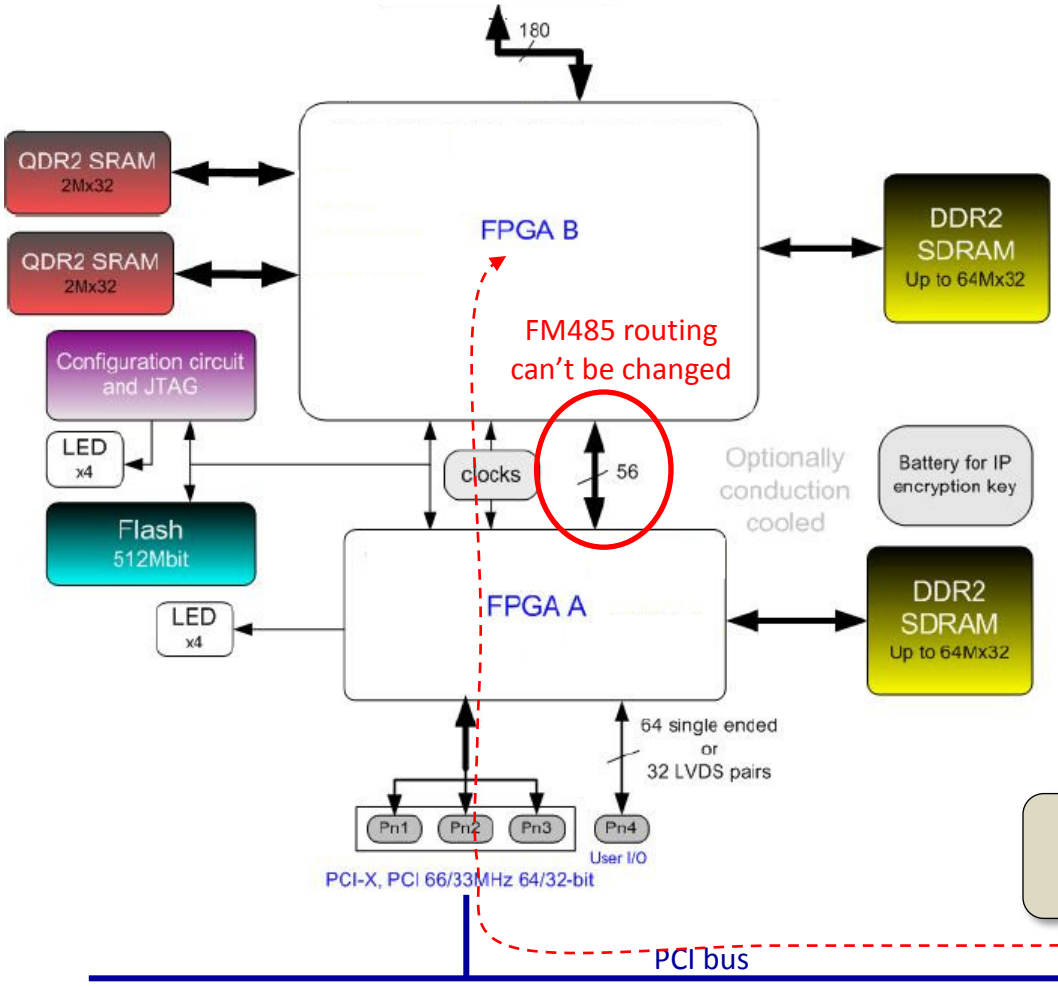
# Design status history

ADC250
daughter board

**Question** : is it possible to use the existing lines between FPGA A and B to R/W user parameters from CPU ?

➡ It means, the only way is to modify/customize the VHDL code

**Answer seems** : yes, it's possible (MISH)
**But** : no specification defined yet
**Conclusion** : meeting required !




Computer
DELL Precision T7500

User Interface program is running on the CPU

*Parameters path*


**VisualStudio 2010**

# Exhanges history

| Questions | 4DSP/MISH Answers | Status |
|---|---|---|
| To MISH 2012.01.25<br>*translated from japanese*<br><br>Dear MISH International,<br>I have some questions about VHDL. On the attached file page 1, I have represented the default design which is a low pass filter (FIR) installed in channel A. But this USER_BLOCK is limited. For my design, I required that the output of the USER_BLOCK is directly connected to DAC and not feed to the HDD. Please see page 2.<br><br>**I have some questions :**<br>1. Do you have such design page 2 ?<br>2. If not, could you provide us this new design ?<br>3. If not, do you have a top schematic version of ADC250_IO.VHD ? | From MISH 2012.01.25<br>*translated from japanese (summerized)*<br><br>The implementation to USER_BLOCK was developed by us. It is aimed for users who don't use VHDL but instead use MATLAB. We sell it as an adaptation package for FM485/ADC250. Therefore, this USER_BLOCK is limited.<br><br>Therefore, the users need to modify /customize the design by themselves. The other way is to send a development request to us, but it will not be free.<br><br>MISH does not have the schematic version of the top design. | OK |

# Exhanges history

| Questions | 4DSP/MISH Answers | Status |
|---|---|---|
| To 4DSP Forum 2012.01.26<br><br>Hello,<br><br>I'm using a FM485 board with an ADC250 (2 channels ADC, 2 channels DAC) daughter board. My lab is in Japan / Hiroshima University.<br>I am working with the MATLAB/SIMULINK Sysgen design flow, associated to XILINX ISE for generating the bitstream and .hex file. Then, I configure the FPGA_B with 4FM software.<br>(Please notice that I don't modify FPGA_A).<br>To do that, I got from MISH company (4DSP distributor in Tokyo) a specific file adc250_io.vhd containing a USER BLOCK.<br>This user block is representing the I/O of the MATLAB/SIMULINK/SYSGEN model.<br>My present model acquires the ADCA input, and after some treatments (native XILINX blocksets and Blackboxes associated to specific VHDL files that I have written) provides an output signal to DACA.<br>It works very well.<br>For the treatments, I need to use parameters. Presently, these parameters are CONSTANTS in the model. Therfore, I have no possibility to change them AFTER generating the FPGA bitstream.<br>For me, this is NOT convenient (regarding my application).<br>Thus, I need to MODIFY the parameters in the FPGA without re-generating the bitstream.<br>So, I need to modify the model so that it accepts parameters on its input. And I intend to change in realtime the parameters with a C software/interface running on the CPU of my computer, using the 4DSP libraries (Board Support Package).<br>QUESTIONS :<br>----------<br>1- If I change the USER_BLOCK.vhd component I/Os, for instance I add a 32 bits std_logic_vector (I think one 32 bits std_logic_vector will be enough for me), this new input has to be connected to ADC250_IO i/o ring. But, this module does not have any "custom" input (nor output, by the way). So, if I add my std_logic_vector to ADC250_IO module, I also need to modify FM485_FPGA_B_ADC250.vhd. Will it be enough ? I mean, can we access this new data from the CPU ? Or, do we also need to modify FPGA_A ?<br>2- Now, we don't have any schematic view for the FM485_FPGA_B_ADC250.vhd. I don't have any tool like ModelSim, so it's very difficult to manage the behavior of FM485_FPGA_B_ADC250.vhd. Do you have an ISE project with a schematic view of the top file ?<br>3- In the 4DSP documentation, you mention Custom Registers. I would like to use these registers because I think I can use them to read/write the parameters. Is it possible ? Where are connected these registers in the FPGA ? Are they connected to FPGA_A or FPGA_B ?<br>Now my situation is the following :<br>1- I can implement my design in the User Block, allowing me to use XILINX blocksets and Simulink environment capabilities.<br>2- I cannot change the parameters of my design. Modifying the parameters in real time is a strong requirement for my design.<br><br>Thanks for your help. I hope to receive your answers very soon.<br><br>Mr. Yoshitama<br>Hiroshima University | From 4DSP Forum 2012.01.26<br><br>Dear Sir,<br><br>all support is channeled through Mish. Could you please contact them in this regard?<br><br>Thank you<br>Pierrick | OK |

# Status / Requests

## 1- Status

1.1- When we ask 4DSP, they tell us to contact MISH

1.2- We have asked MISH and answer is the following :

1.2.1- the USER_BLOCK is intended for customers who don't use VHDL design but MATLAB/SIMULINK

1.2.2- the users need to modify/customize the design according to their need.

**Comment** : The User_block is intended to users who do not use VHDL but Simulink model, but the modification according to our need requires to **modify the VHDL code** ! Conclusion : point 1 and point 2 are **not consistent**.

1.2.3- MISH can develop our required design, but not for free.

## 2- Request

2.1- If we want to comply to point 1.2.2 above, what are the information **we must have** to be able to customize the MISH design ?

Comment : if we don't have these information, there's no need to try to modify the present design by ourselves. **Conclusion** : the only solution is to pay for a MISH develoment !

2.2- If we agree to ask MISH for a new design, can we meet as soon as possible to define our need (*specifications*) ?

2.3- what would be the cost and delay of the new design ?