R&D STATUS OF CCD BASED VERTEX DETECTOR FOR JLC *

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Abstract

One of the goal of our study is to operate a CCD vertex detector at near room temperature, in order to reduce materials of cooling system and minimize a thermal distortion of sensor. In this article, the current status of our R&D is described, which is mainly concentrated on the radiation damage issues at near room temperature.

1 Introduction

The CCD based vertex detector is one of the best candidates for future linear collider. The small size of pixels gives an excellent spatial resolution, and the large chip size is available. Usually, normal CCDs have wafer thickness of about 500μm, while the thickness of sensitive region is only about 20μm in the wafer. For the use as the vertex detector, the insensitive substrate should be thinned as much as possible to reduce the multiple scattering of charged particles. On the other hand, it is more difficult to keep such thin silicon wafers flat particularly operated at

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low temperature[1] due to thermal distortion. If the temperature becomes lower, it might cause mechanical destruction of thin wafer, or large systematic errors in the alignment, so that the operation at near room temperature (∼0°C) is desirable.

The first step of our study effort was devoted to test several types of CCD structures with Multi Pinned Phase (MPP) operation[2]. From those studies, we have confirmed that MPP operation suppress the dark current effectively, and the signal-to-noise ratio (S/N) is above 10 for minimum ionizing pions, even at +5°C with the readout cycle of 3 seconds. It is noted that S/N is improved by the reduction of thermal noise, if the faster readout cycle was performed. We have achieved the intrinsic resolution is better than 3μm at -15°C[3]. The radiation damage has been studied by irradiating CCD samples using the radio isotopes, ^{90}Sr and ^{252}Cf for electrons and neutrons, respectively. The serious problem of radiation damage is a increase of the charge transfer inefficiency (CTI). We have measured the CTI at readout cycle of 3 seconds. The CTI for irradiated CCDs has been improved by the concentration of signal charge that was performed using 2-phase clocking, notch structure and fat-zero charge injection[3, 4]. If we assume the limitation of vertical CTI (VCTI) is less than 10^{-3}, CCDs can be used up to $1.5\times10^{12}/\mathrm{cm}^2$ electron irradiation at near room temperature. It is known, however, that the bulk damage by minimum ionizing electron is about 10 times stronger than low energy electrons. The experimental confirmation of the radiation damage for high energy electron is one of the important issue. The limit of the CCD against neutron background is deduced as $1.5\times10^{10}/\mathrm{cm}^2$[5].

Second stage of our R&D program have to be carried out at more actual operating condition. In the JLC, the CCDs are read out every train crossing of 6.7ms. Each CCDs have multiport readout node, so that the readout frequency will be a few ×10 Mpixels/s. This faster readout condition will reduce the thermal noise to negligible level, while it will make VCTI increase by the lack of sacrificed thermal charge which fills up defect state at near room temperature. The more precise study of background condition in the JLC is also necessary, in order to study radiation damage at more actual background condition. In this article, we introduce a current status of our R&D for continuous study of radiation damage at more similar condition to the JLC experiment. Those are development of fast readout system, precise background study, and irradiation experiment by high energy electrons.

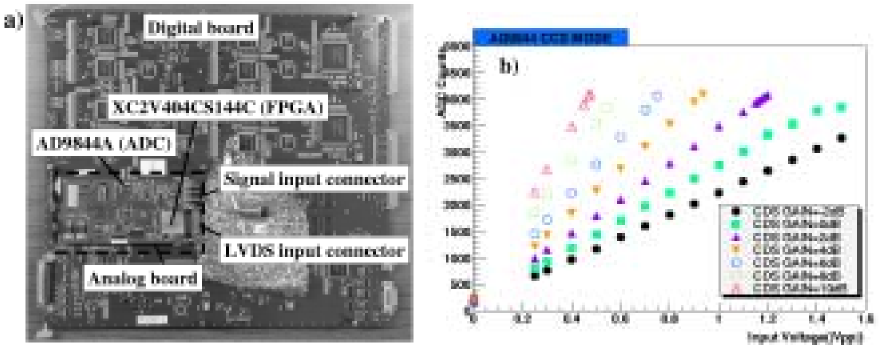

Figure 1: a)Analog board with AD9844A ADC sit on the digital board, and b)linearity curve of ADC9844A for various CDS gain settings.

2 Fast readout system

The fast readout module has been designed and fabricated as a prototype. The module consists of the digital board and analog board as shown in Fig.1 a). The analog board includes an analog-to-digital converter (ADC) chip and a FPGA which supplies the drive clocks to ADC. The clock pattern is loadable via LVDS interface. The signals are digitalized on analog board and sent to the digital board via backplane connector. The digital board has a interface of CPCI(6U) for the operation of the data acquisition computer. For the ADC, we used a commercially available 9mm×9mm CCD signal processor chip for digital camera, AD9844Amanufactured by Analog Devices Co. The cost is only about \$6 US/chip. The feature of AD9844A is 12 bit 20MSPS ADC with correlated double sampling (CDS) and low power consumption (6mW/2.7V). The CDS gain is adjustable in 6 bit resolution. Fig.1 b) shows measured linearity curves for various CDS gain settings.

3 Background study

The main source of background for the vertex detector is e^+e^- pairs which come from the beamstrahlung process during collisions. The hit density for this process was simulated with detailed geometries by the JUPITER[6] full detector simulator,

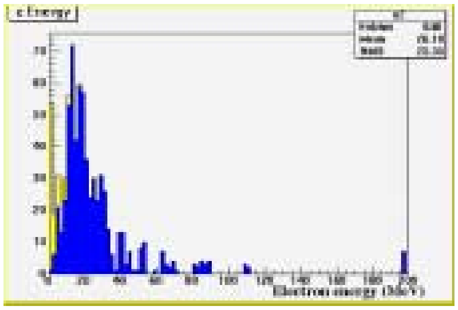

Figure 2: The energy distribution of e^+e^- pairs background at the vertex detector for TRC(X)[8] beam parameter, where hatched area represents direct contribution of e^+e^- pairs.

where beamstruhlung process is calculated using CAIN package[7]. Fig.2 shows the energy distribution of electrons and positrons which hit the vertex detector, where low energy electrons are produced by the delta ray or conversion processes at the silicon sensor. The energy of the electron is about 20 MeV at the most probable value. The estimated hit density at the inner most layer at the radius of 24mm, is $0.5\times10^{11}/\mathrm{cm}^2$/year, where the detector magnet of 3 Tesla was assumed.

4 Irradiation of High energy electron

Non Ionizing Energy Loss (NIEL) hypothesis[9] predicts 10 times larger radiation damage for minimum ionizing particle than that for ^{90}Sr β-ray. Our background simulation shows the most probable energy of electrons is about 20 MeV, so that the effect of radiation damage should be measured experimentally.

We have proposed the electron irradiation experiment using high energy electron beam at Laboratory of Nuclear Science (LNS) at Tohoku university. Fig.3 shows the experimental setup of the electron irradiation. We use tagged photon beam line, and irradiate CCDs with the electrons recoiled at the Platinum radiator. The momentum of electrons is separated spatially using bending magnet. CCDs are laid with does monitors, those are RADFET (REM CC-5) for accumulated dose monitor, and PIN photo-diode array for intensity and profile monitor by the leakage

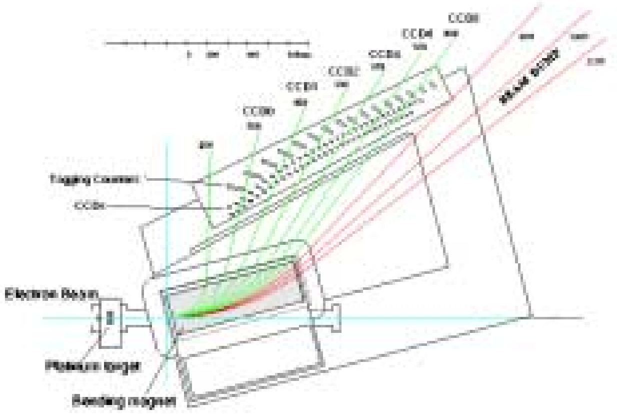

Figure 3: Experimental setup for irradiation test

current measurement. Fig.4 shows an expected momentum distribution of electron which irradiate CCDs. The momentum range covers actual situation of e^+e^- pairs background in the JLC. The type of irradiated CCD is a 2-phase buried channel CCD with the maximum readout frequency of 10 Mpixels/s, manufactured by Hamamatsu Photonics K.K. The characteristics of irradiated CCD will be investigated using fast readout system for dark current, flat-band voltage shift, CTI, and spatial resolution, as we have already performed in the previous studies.

5 Summary

The current status of our studies for the JLC CCD vertex detector is reported. The studies are concentrated on the radiation damage at more actual background condition and at fast readout operation in the JLC.

The precise study of background is in progress using newly developed JUPITER simulator with precise geometries. Newly developed readout system has been designed and fabricated. The proposal of radiation damage experiment by high energy electron has been approved, and the irradiation will be repeated up to $10^{12}/\mathrm{cm}^2$

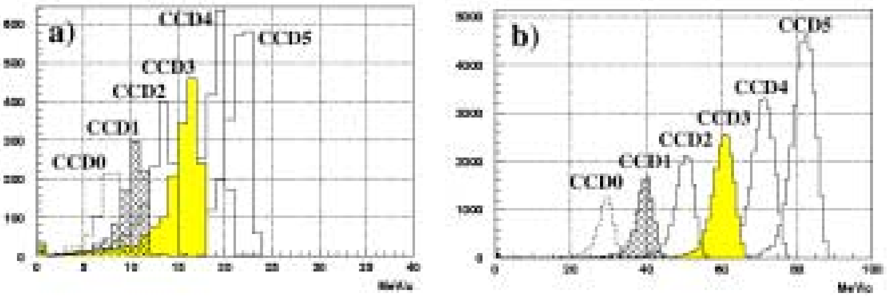

Figure 4: Expected momentum distribution of electrons for the setting of beam energy, bending magnet, thickness of radiator, a)60MeV, 0.114Tesla,0.1X_0, and b)125MeV, 0.428Tesla, 0.1X_0, respectively.

electrons in 2003 physical year, which correspond to more than 10 years operation in the JLC.

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