Development of FPCCD Readout ASIC

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Introduction

FPCCD vertex detector

- Pixel size: 5µm
- Thickness: 15µm
- Signal level: <2000e
- Readout channel: 16 or 32 ch
  - ~20,000 x 128 pix/ch

Test-sample was delivered in Mar., 2008.

- Pixel size: 12µm
- Readout channel: 4ch
  - 512 x 128 pix/ch

Development of the readout ASIC was started.
Requirement to the readout ASIC

- All elements to read from FPCCD are contained in one chip.
- Readout rate: >10 Mpix/sec
  - [20000 x 128 pix]/[0.2 s]
- Noise level of the ASIC: < 30 electrons
  - Required total noise level including the CCD: <50 electrons
  - Noise level of FPCCD: ~30 electrons
- Power consumption: < 6 mW/ch
  - The power consumption in a cryostat should be <100 W.
  - Required total power consumption: <16 mW/ch (~100W/6000ch)
  - CCD: ~10mW/ch

To achieve these requirement, readout ASIC was designed.
Design concept of readout ASIC

ASIC elements

• Voltage amplifier
• LPF (Low-pass filter)
• CDS (Correlated double sampling)
• ADC
  ➢ 2 charge sharing ADC are used alternatively to achieve 10Mpix/sec.
• LVDS driver

From CCD → Voltage amplifier → LPF → CDS → Charge-sharing ADC (6bit) → LVDS driver

Serial output

FPC CD

V_{sig}
Expected performance

• Readout rate : 10 Mpix/sec → OK!
  ➢ Data conversion rate : 10MHz (= 5x2 MHz)
  ➢ 260 ms/ch : [20000 x 128 pix/ch] x [10⁻⁷ s/pix]
• Power consumption < 5 mW/ch → OK!
  ➢ Charge-sharing ADC realizes low power. (~10 μW)
• Noise level : ~10e → OK!
  ➢ Estimation with SPICE simulation.

The performance will satisfy our requirement.

The prototype of the readout ASIC was produced.
Readout ASIC

Readout ASIC prototype

• The readout ASIC was delivered in Jan., 2008.
• The chip was produced by MOSIS.
  ➢ Size : 2.85 x 2.85 mm²
  ➢ # of pad : 80
  ➢ Readout channel : 8
• The chip was covered by QFP-80pin package.

Readout system was constructed to perform the response test.
Readout system

- Operation and data-acquisition is done by VME-GPIO module.
- ADC serial pulse is analyzed by a FPGA on the GPIO module.
- The ADC information is sent to PC.
Picture of readout system
Internal signals in the readout ASIC were checked by the monitor output.

- The monitor is prepared after amplifier and before ADC.
- All monitor output was observed.

→ The amplifier, LPF, and CDS are working.

ADC output was checked.
Output signals from the ADC were checked.

- ADC output: sign-bit + 6bit (: -64~+64 ADC-count)
- The ADC values are read successfully.

→ The performance was studied with 1.5 Mpix/sec readout rate.
The noise level of the prototype ASIC was checked.

- Some ADC counts are not output due to precision of the MSB (Maximum Sensitive Bit) capacitor.
- The problem will be fixed in the next production.

Noise level in FPCCD: 40e

- Requirement: <30e
- \( \sigma : 1.0\text{ADC} \)
  - 1 ADC = 0.2mV for sensor input
  - 5\( \mu \)V/e in FPCCD

The noise level was almost acceptable.
The ADC linearity was checked, fitting with a linear function.

- The linearity was within $\pm 80e$.
- The ADC linearity will be improved after modification of the MSB capacitor.
Problem in high rate readout

Some efforts are necessary to readout with 10Mpix/sec.

• Fluctuation of the baseline voltage for ADC becomes larger.
  ➢ The ADCs do not work correctly.
• The noise on the power line must be reduced.

ADC distributions for the pedestal

1.5Mpix/sec

5Mpix/sec
Summary

• The readout ASIC for FPCCD was developed in 2008.
• Some ADC count are not output due to the precision of the MSB capacitor.
• The performance of the readout was performed with 1.5 MHz readout rate.
  > The noise level : 40e
  > The ADC linearity : ±80e.
• The ADC distributions broaden for higher readout rate (5Mpix/sec).
  > The noise on the baseline voltage must be reduced.