Development of FPCCD Readout ASIC

’08 3/5  Y. Takubo
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FPCCD vertex detector

- Pixel size: 5μm
- Thickness: 15μm
- Signal level: ~500e for large angle
- Readout channel: 16 or 32 ch
  - ~20,000 x 128 pix/ch

Test-sample will be delivered in 2008.

- Pixel size: 12μm
- Readout channel: 4ch
  - 512 x 128 pix/ch
Motivation to develop readout ASIC

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• The FPCCCD test-sample will be delivered in the end of this year.

• The FPCCCD has a large number of readout pixels.
  ➢ Test sample: 512 x 128 pix/ch

• There is no readout ASIC suitable for the FPCCCD.

Readout ASIC for the FPCCCD is necessary.

• For FPCCCD test-sample
• To establish readout technique
Requirement to the readout ASIC

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• All elements to operate and read FPCCD are contained in one chip.
• Readout rate : >10 Mpix/sec
  ➢ [20000 x 128 pix]/[0.2 s]
• Noise level of the ASIC : < 30 electrons
  ➢ Required total noise level including the CCD : <50 electrons
  ➢ Noise level of FPCCD : ~30 electrons
• Power consumption : < 6 mW/ch
  ➢ The power consumption in a cryostat should be <100 W.
  ➢ Required total power consumption : <16 mW/ch (~100W/6000ch)
  ➢ CCD : ~10mW/ch

To achieve these requirement, readout ASIC is designed.
Design concept of readout ASIC

ASIC elements

- Voltage amplifier
- LPF (Low-pass filter)
- CDS (Correlated double sampling)
- ADC

- 2 charge sharing ADC are used alternatively to achieve 10Mpix/sec.

- LVDS driver

The design was optimized with SPICE simulation.
Design optimization with SPICE

- The SPICE simulation was applied to design the readout ASIC.
- The design was optimized for 0.35 μm process by TSMC.

Logic design of the readout ASIC

Logic design of the readout channels

Each element was checked with simulation.
Expected performance

- Readout rate: 10 Mpix/sec → OK!
  - Data conversion rate: 10MHz (= 5x2 MHz)
  - 260 ms/ch: [20000 x 128 pix/ch] x [10^{-7} s/pix]
- Power consumption < 5 mW/ch → OK!
  - Charge-sharing ADC realizes low power. (~10 μW)
- Noise level: ~10e → OK!
  - Estimation with SPICE simulation.

The performance will satisfy our requirement.

The prototype of the readout ASIC was produced.
Readout ASIC prototype

- The layout was made by Digian technology.
- The chip was produced by MOSIS.
  - Size: 2.85 x 2.85 mm²
  - # of pad: 80
  - Readout channel: 8
- The chip was covered by QFP-80pin package.

Test-bench was constructed to perform the response test.
VME-based system was developed for the test-bench.

- Operation and data acquisition is done by VME-GPIO module.
- Response of the readout ASIC was checked, connecting to GPIO.

**Block diagram of test-bench**

FPCCD test-board

ASIC test-board

ASIC

VME-GPIO

PC

Signal

Data : 8ch

Operation signals

Reset

Shift clocks
Test bench

Operation board (GPIO)

Test-board

Readout ASIC
Response test

Test menu

• Monitor output
  ➢ After gain-amplifier
  ➢ Differential signal before ADC
• Gain adjustment
• ADC output

The response test was performed.
Analog monitor output

Monitor output was checked at the timing of test-pulse.

• All monitor output can be observed.

→ The amplifier, LPF, and CDS are working.

Response of adjustment block for gain was checked.
Gain adjustment

The monitor output was checked, changing the amplifier gain.

• Adjustment of the gain is done by the operation signal from outside.
• The pulse height could be changed by the setting the gain.

→ The adjustment block for the amplifier gain is working!
ADC output

The output from ADC was checked.
• Serial output from ADC was confirmed.

→ All components in the readout ASIC is working!

The next step is to investigate the performance.
Summary

• The readout ASIC for FPCCD was developed.
• Response test of the readout ASIC was started.
• The output of analog monitor was checked.
  ➢ The amplifier, LPF, CDS are working.
  ➢ The amplifier gain can be adjusted by the operation signal from outside.
• The serial output from ADC was confirmed.
• All components in the readout ASIC are working.
• The next step is performance study.