FADC for VTX Readout

Kazuo Nakayoshi
(KEK Online)

On behalf of VTX Group
Outline

• Introduction
• CCD Signal Processor
• New Readout System
  – cPCI-based Readout System
  – New DAQ Platform @KEK
• Summary
Introduction

• For study of CCD Clock dependence on
  – CTI (Charge Transfer Inefficiency)
  – DCP (Dark Current Pedestal)
  – Hot pixels

• Performance of current readout system is not good enough (2MB/sec).

We need a High-speed (20Mpix/sec) readout system.
CCD Signal Processor AD9844A

- Features
  - 20MSPS Correlated Double Sampler (CDS)
  - 12Bit 20MSPS A/D Converter
  - 3-Wire Serial Digital Interface
  - Low Power: 65mW
  - Low Cost

- Applications
  - Digital Still Cams
  - Digital Video Cams
CCD Signal Processor AD9844A

- Correlated Double Sampler (CDS)

- Internal Register
CCD Signal Processor AD9844A

• AUX1 Mode

• AUX2 Mode
**cPCI Readout System**

- cPCI FADC(AD9844A) Niigata, KEK, RINEI
  - 4ch CCD Input
  - External 3 clocks (LVDS)
  - 1Mwords Memory/ch
- CPU (Sanritz Automation)
  - Pen4-M 2.2GHz
  - ServerWorks GC-LE
  - 1000Base-T 2ch, 100Base-Tx 2ch
- Crate(EBRAIN)
  - 5Slots
Status of cPCI Readout System

- Digital Part test: Done @KEK
- Device Driver: Done @KEK
- Integrated test: Resuming @Niigata Univ.
  - AUX1 mode Test: Done
Issues of dPCI FADC

- The current version of FADC cannot be operated with DMA transfer mode.
- We have to add DMA transfer logic to it for high-speed readout.
- It will take a good amount of time to complete.

Another Solution?
New DAQ Platform @KEK

- **COPPER** (COmmon Pipelined Platform for Electronics Readout)
  - PCI bus based Mother Board (9U VME)
- **FINESSE** (Front-end INstrumentation Entity for Sub-detector Specific Electronics)
  - Simple designed I/O card
- **PMC Processor** (Pen III 800MHz, Linux 2.4.x)
- **KEK VME Crate 9U**
FINESSE

2ch 500MHz FADC

8ch 65MHz FADC

24ch TMC TDC

2ch 20MHz CCD FADC

Developed by K. Tauchi@KEK Elec. Group

4 March 2005

ILC Detector Workshop@KEK
Processor PMC

RadiSys EPC-6315

- RadiSys 82600 Chipset
- 800MH zPentium III-M
- 32bit 66MHz PCI I/F
- 10/100 Base T Ethernet
- CompactFlash

OS: Linux(2.4.x)
Test Bed

FINESSE(FADC)
FINESSE CCD-FADC Prototype

AD9844A

FPGA(Spartan-3)
FINESSE CCD-FADC Prototype

Diagram of the FINESSE CCD-FADC Prototype with various components and connections. The diagram shows the flow of signals from the CCDIN, EX. CLK, EX. GATE, and other inputs to the AD9844A, Serial I/F, I/O Reg., and SYNC FIFO, with outputs going to Event FIFO and To Event FIFO.
FADC AUX1 Mode Test

CCD CLK: 20MHz
Input: 27kHz, 340mV
FADC AUX1 Mode Test

Number of Events

CLK : 10MHz
Input : 0mV

Entries : 13412
Mean : 2055
RMS : 1.464
$\chi^2$/ ndf : 129.7 / 2
Constant : 7415 ± 77.84
Mean : 2055 ± 0.01302
Sigma : 1.429 ± 0.00848

4 March 2005  ILC Detector Workshop@KEK
FADC CCD Mode Test

Graph

Input Signal (V)

ADC Data

0 0.2 0.4 0.6 0.8 1 1.2 1.4

Very Preliminary
Status of FINESSE FADC

- Logic Programming: *Almost Done*
  - CCD 3 CLOCKs
  - Serial Interface
  - I/O Register
  - FIFO
- PIO read Test: *Done*
- AUX1 mode Test: *Done*
- CCD mode Test: *Going*
Summary

• We are working to build High Speed Readout System for study of CLK dependence on CTI, DCP, Hot Pixels.
• We have two options;
  – cPCI based Readout system
  – New DAQ Platform
• Now testing FINESSE-FADC Prototype
  – PIO read from COPPER’s Event FIFO was checked out
• Resumed cPCI FADC work @Niigata Univ.
Schedule

- Finalize the logic programming of FINESSE FADC
  => By the end of March
- Test using real CCD signals
- High-Speed readout test using DMA transfer on COPPER
  => March - April
- Resume dPCI FADC work @KEK
  => April - May?