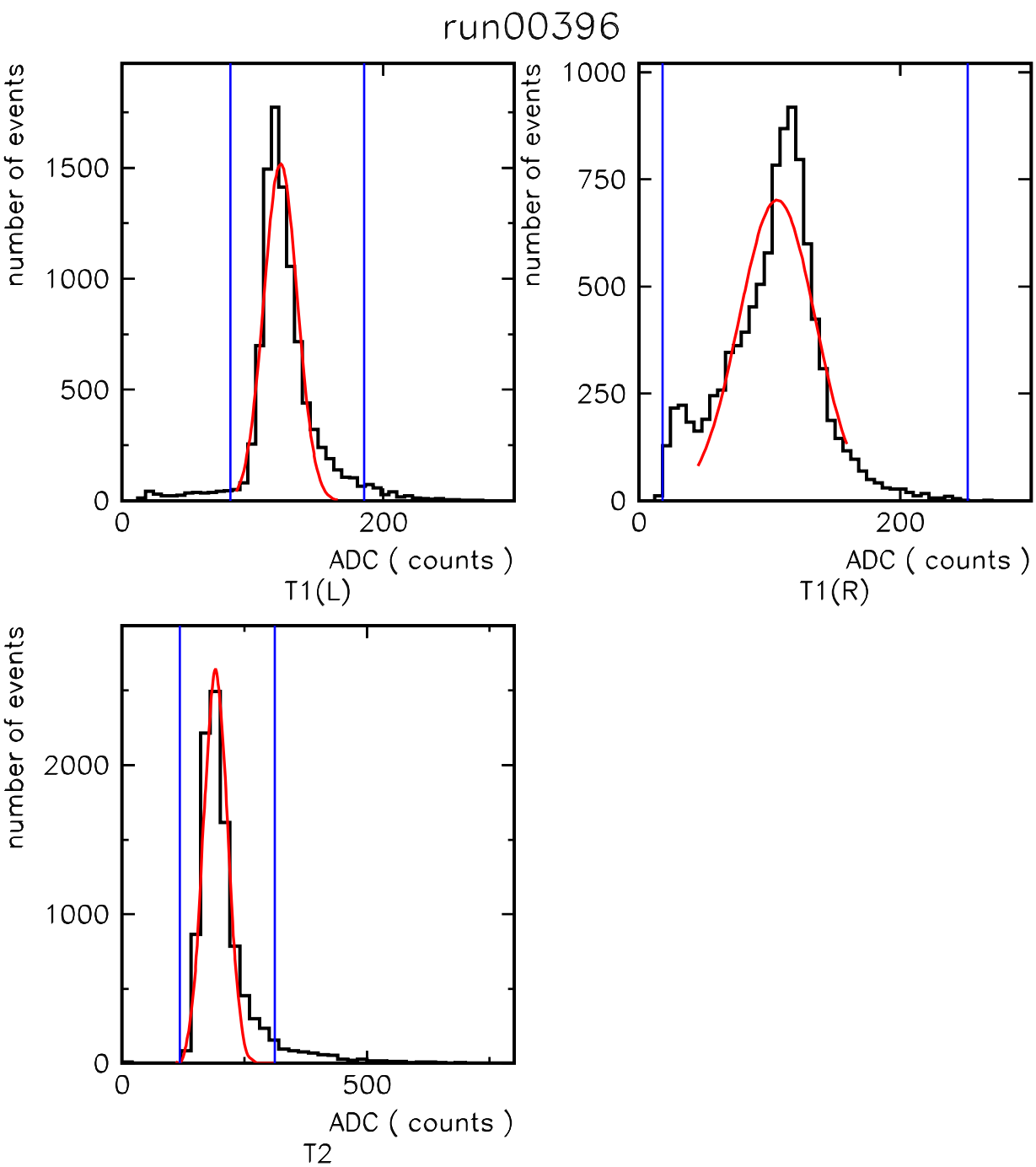
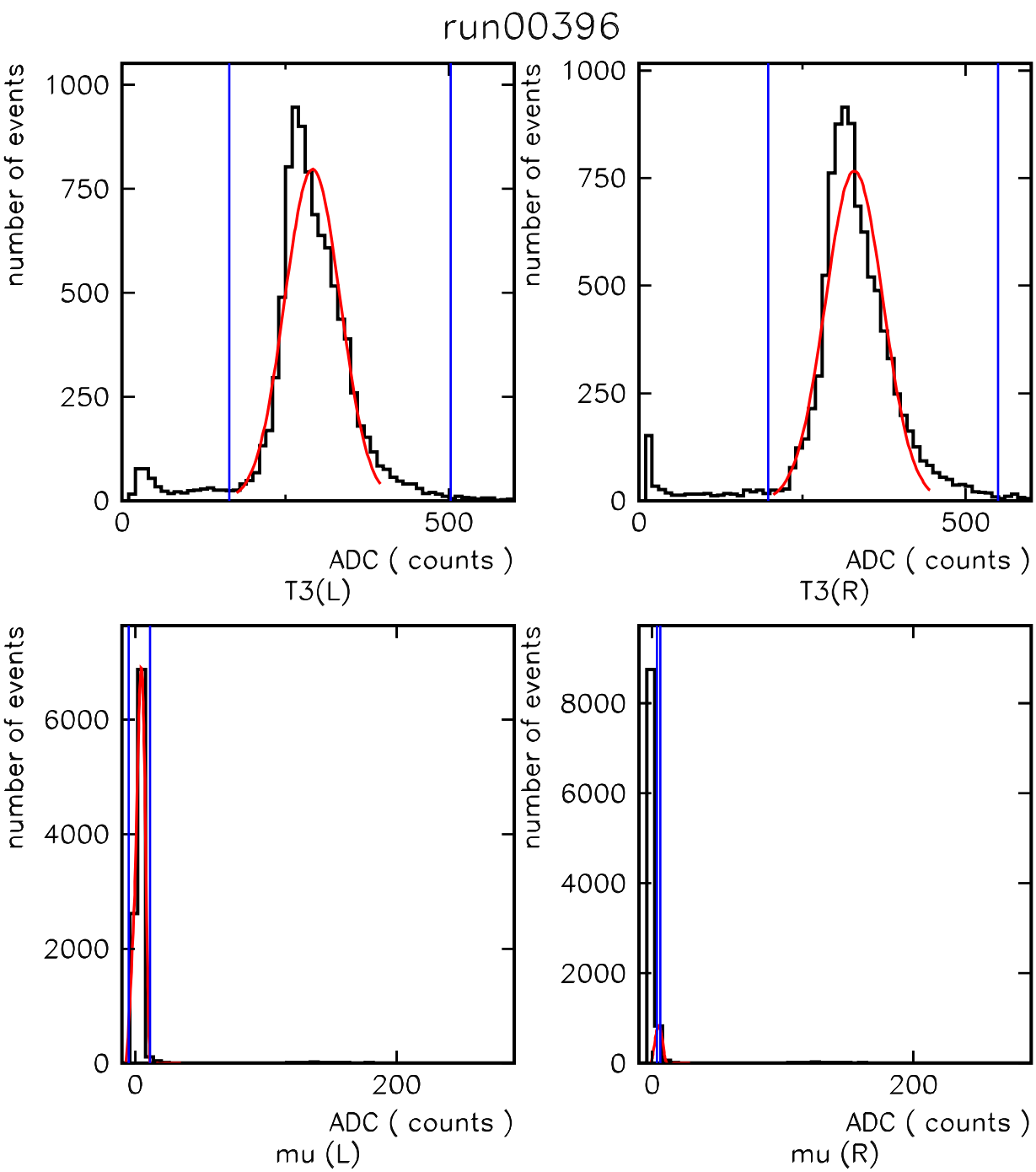
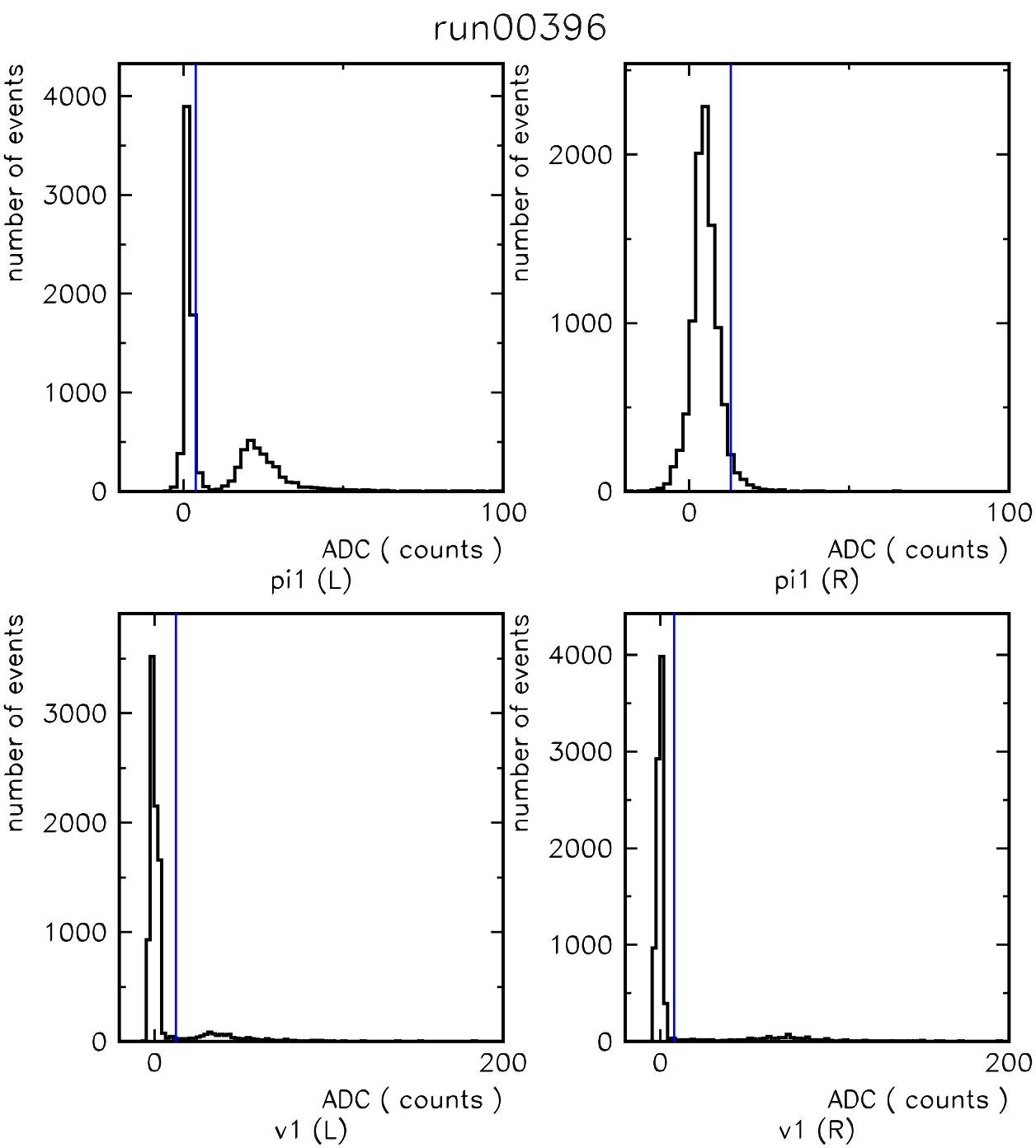
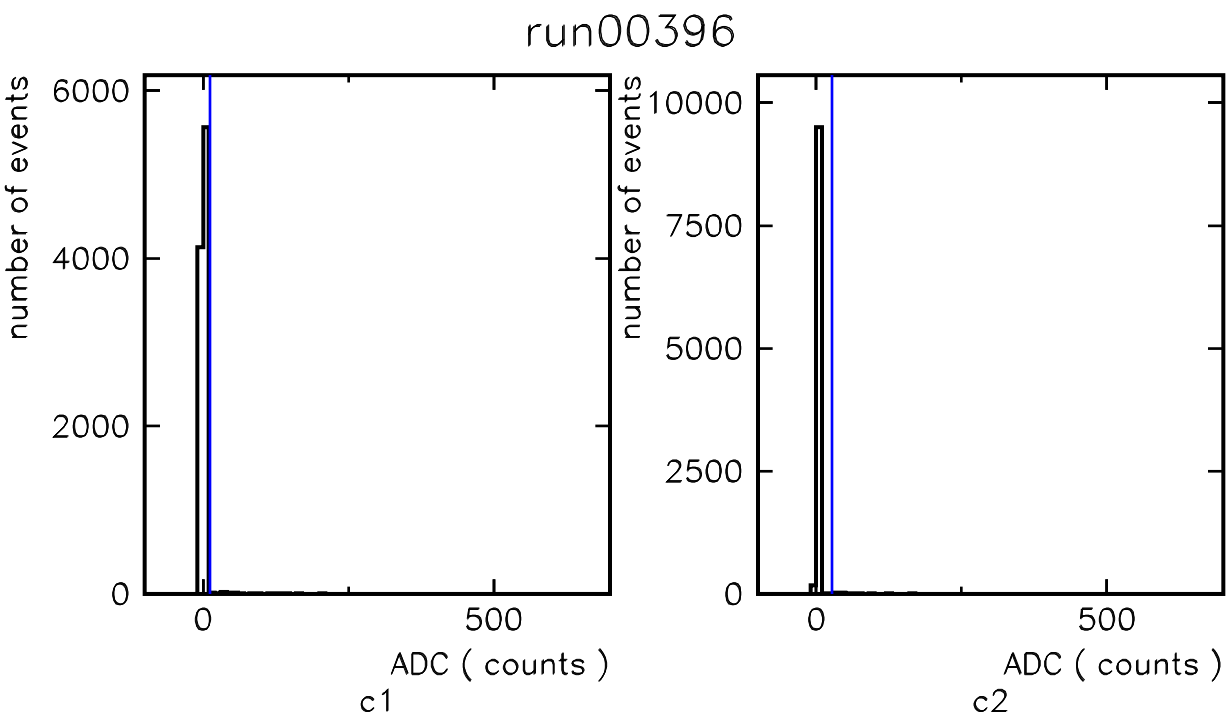

run00396
number of events
1500
1000
500
0
0
200
ADC (counts)
T1(L)
number of events
1000
750
500
250
0
0
200
ADC (counts)
T1(R)
number of events
2000
1000
0
0
500
ADC (counts)
T2


run00396
number of events
1000
750
500
250
0
0
500
ADC (counts)
T3(L)
number of events
1000
750
500
250
0
0
500
ADC (counts)
T3(R)
number of events
6000
4000
2000
0
0
200
ADC (counts)
mu (L)
number of events
8000
6000
4000
2000
0
0
200
ADC (counts)
mu (R)


run00396
number of events
4000
3000
2000
1000
0
0
100
ADC (counts)
pi1 (L)
number of events
2000
1000
0
0
100
ADC (counts)
pi1 (R)
number of events
3000
2000
1000
0
0
200
ADC (counts)
v1 (L)
number of events
4000
3000
2000
1000
0
0
200
ADC (counts)
v1 (R)


run00396
number of events
6000
4000
2000
0
0
500
ADC (counts)
c1
number of events
10000
7500
5000
2500
0
0
500
ADC (counts)
c2