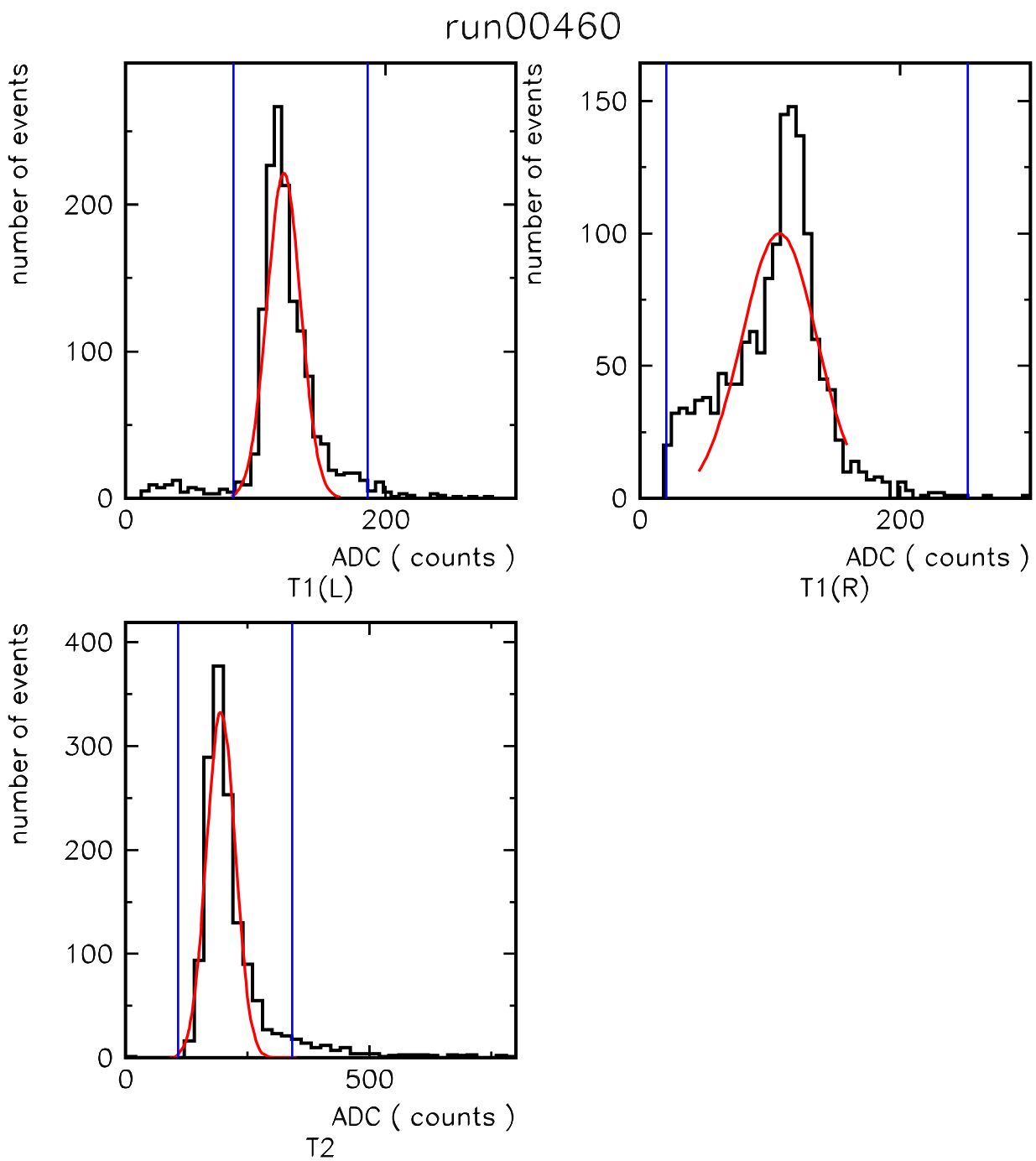
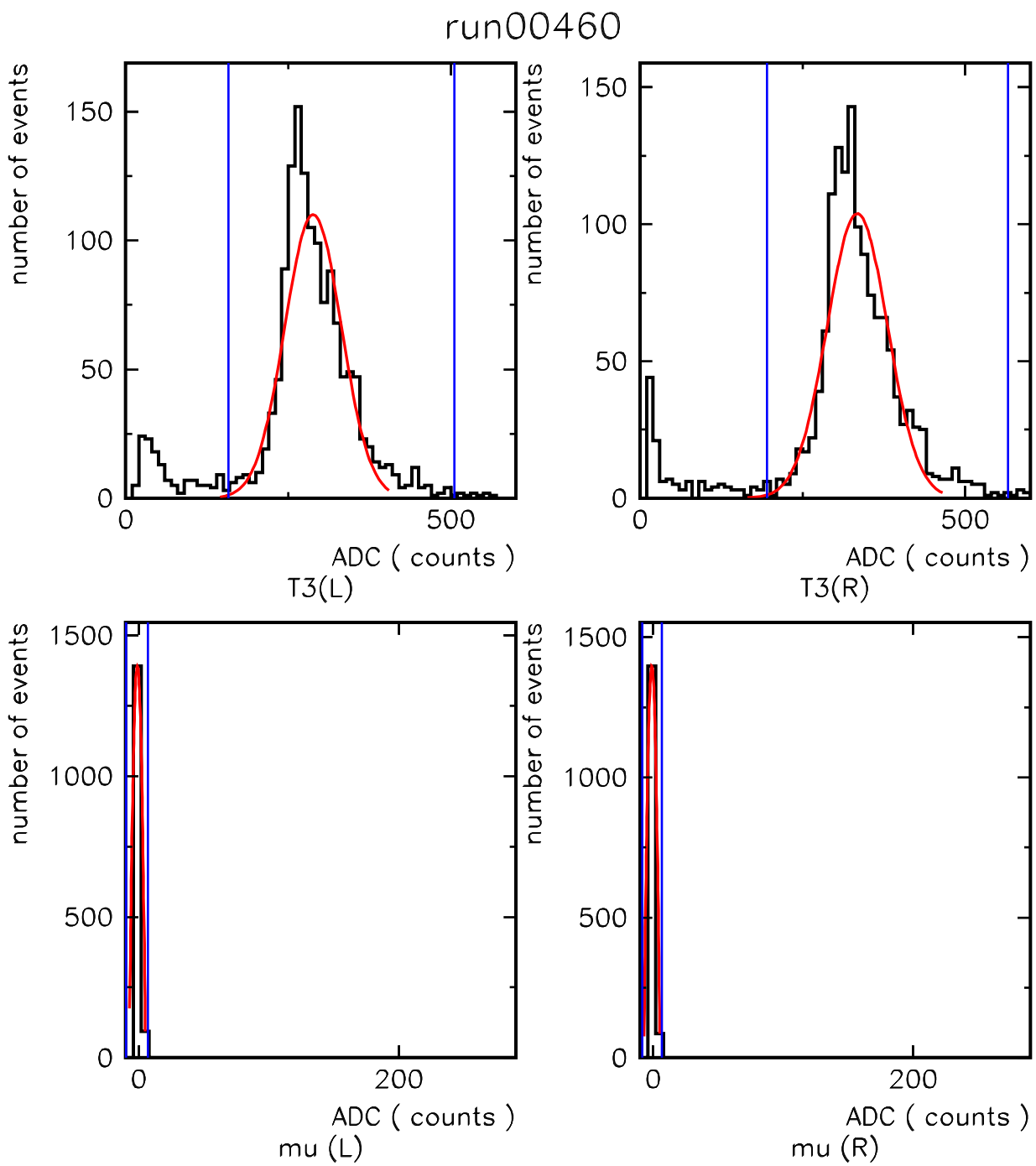
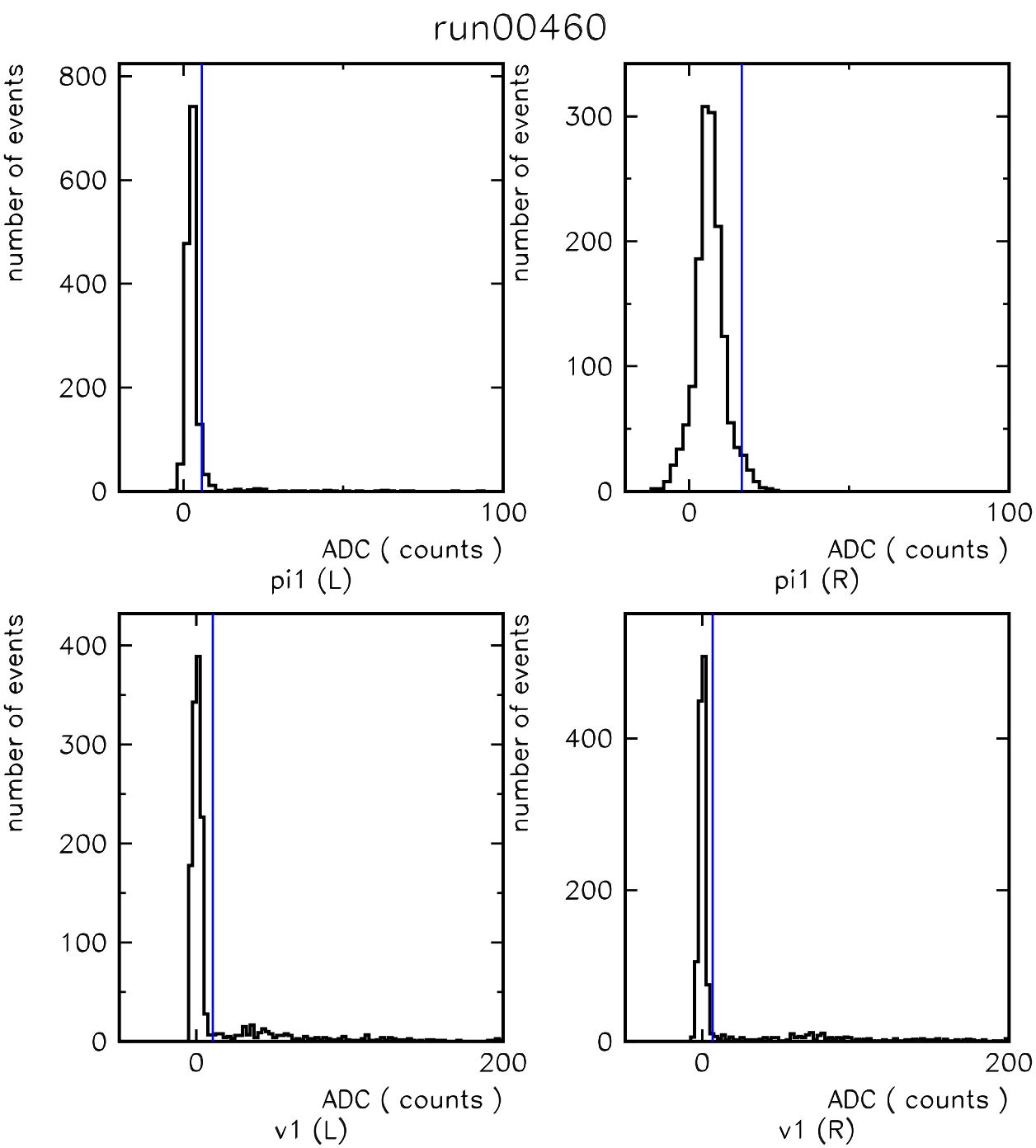
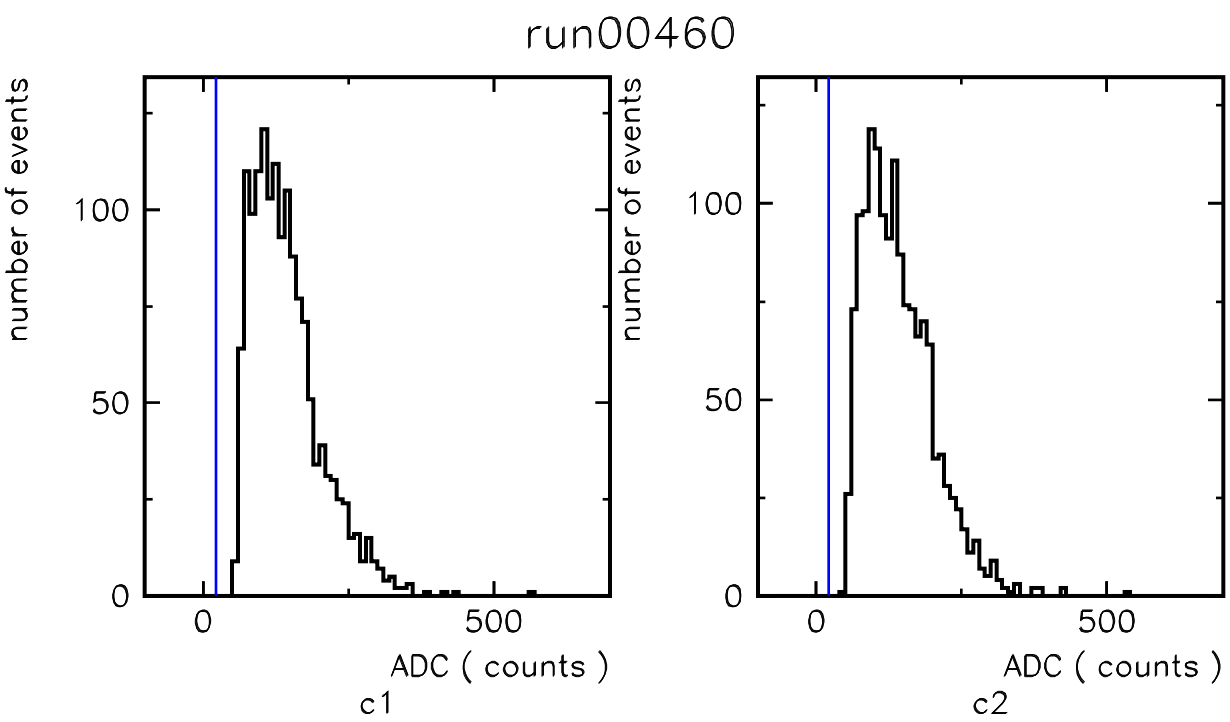

run00460
number of events
200
100
0
0
200
ADC ( counts )
T1(L)
number of events
150
100
50
0
0
200
ADC ( counts )
T1(R)
number of events
400
300
200
100
0
0
500
ADC ( counts )
T2


run00460
number of events
150
100
50
0
0
500
ADC ( counts )
T3(L)
number of events
150
100
50
0
0
500
ADC ( counts )
T3(R)
number of events
1500
1000
500
0
0
200
ADC ( counts )
mu (L)
number of events
1500
1000
500
0
0
200
ADC ( counts )
mu (R)


run00460
number of events
800
600
400
200
0
0
100
ADC ( counts )
pi1 (L)
number of events
300
200
100
0
0
100
ADC ( counts )
pi1 (R)
number of events
400
300
200
100
0
0
200
ADC ( counts )
v1 (L)
number of events
400
200
0
0
200
ADC ( counts )
v1 (R)


run00460
number of events
100
50
0
0
500
ADC ( counts )
c1
number of events
100
50
0
0
500
ADC ( counts )
c2