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Physics Group Report

JLC Vertex Detector Subgroup (by Yasuhiro Sugimoto (KEK))

Schematic view of the present design of the vertex detector put in the JLC full simulator JIM is shown in Fig. 1. The main parameters are as follows:

- four layers of CCDs at $r = 24$, 36, 48, 60 mm;
- angular coverage of $|\cos\theta| < 0.9$;
- wafer thickness of 300 μm;
- pixel size of 25 μm^2;
- spatial resolution of $\sigma = 4$ μm.

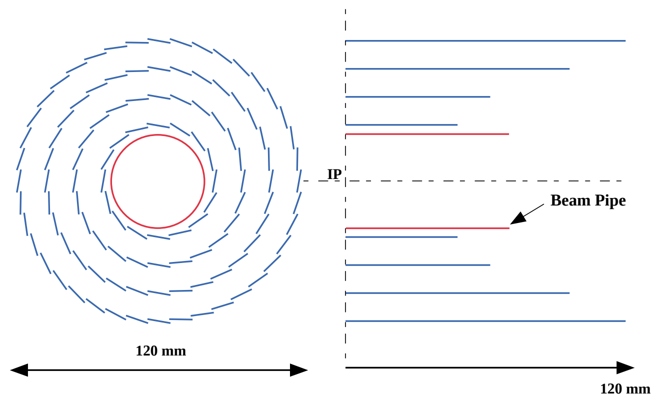

Figure 1: Schematic design of the CCD vertex detector for JLC.

In a simple model of the vertex detector which has two layers at $r_{in} = 24$ mm, $r_{out} = 60$ mm, and other parameters listed above, the impact parameter resolution σ_b can be expressed as

$$\sigma_b = 7 \oplus \frac{20}{p\beta \sin^{3/2}\theta} \ (\mu\text{m}), \tag{1}$$

where p, β, and θ are momentum, velocity, and polar angle of the charged particle, respectively. Actually impact parameter resolution better than equation (1) is obtained by simulation studies because the vertex detector has four layers and the CDC contributes to the improvement of the resolution. At high momentum limit, σ_b of ~ 3 μm is obtained by the simulation, rather than 7 μm given by the first term of equation (1).

So far our major effort of R&D is dedicated to study of radiation hardness of CCDs. Recently, we added new items to our R&D program. Now we briefly discuss on the R&D status and plan.

Spatial resolution: better than 3 μm has been achieved

Spatial resolution is the major concern for vertex detectors. CCDs have excellent spatial resolution by utilizing charge sharing between adjacent pixels. We have confirmed the spatial resolution of better than 3 μm with test beam. Recently a laser beam scanner with 1064 nm wave length and 2 μm spot size has been set up at Niigata University for the study of the spatial resolution of CCD sensors (Fig. 2).

Study of distortion of CCD wafers : challenge for extremely thin detectors

It is desireble to use CCD wafers as thin as possible for vertex detectors to minimize the multiple Coulomb scattering. For detection of chrged particles, 20 μm is enough for the thickness of CCDs. Supporting system of such thin wafers is one of the R&D items of the vertex detector. We are investigating partially thinned wafers as a candidate for the vertex detector. Fig. 3 shows a sample of such kind of wafer. Distortion (non flatness) of the thinned part is one of the concerns. A system of distortion measurement has been constructed.

Figure 2: Laser scanner system for resolution study of CCDs.

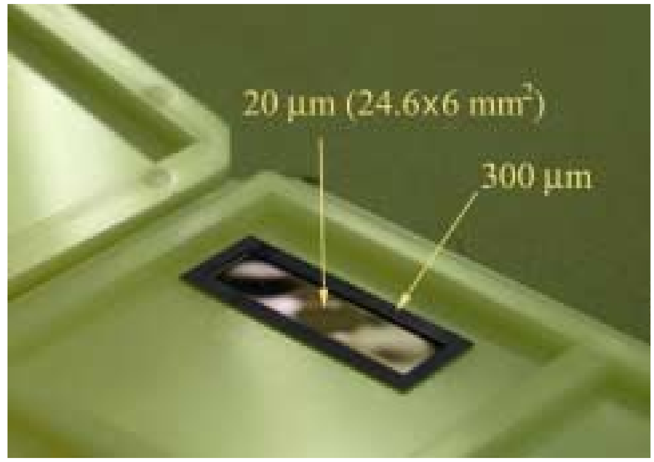

Figure 3: A CCD sample partially thinned to 20 μm.

<u>Radiation hardness of CCDs</u> **: lifetime of 3 years is expected under "A" − should be compatible with "Y" option**

Beam background at the JLC experiment gives radiation damage on the CCD sensors. The damage effect appears as an increase of dark current and charge transfer inefficiency (CTI). We have studied radiation immunity of CCDs using iradiation by ^{90}Sr β source and ^{252}Cf neutron source. Through the study so far, we found techniques to increase the immunity of CCDs, such as "notch channel" and "fat zero charge injection".

Bulk damage by electrons has energy dependence. Because background e^+e^- pairs have haigher energy than ^{90}Sr β ray, we made a naive assumption (NIEL hypothesis) and scaled the results of our study. Then we found that CCDs of the innermost layer ($R_{min} = 24$ mm) can survive more than 3 years with the magnetic field of 2 Tesla and the standard luminosity machine parameter of "A". However it is preferable to have smaller R_{min} and the high luminosity machine parameter option "Y". In order to achiev these options, study of radiation hardness of CCDs should be continued. We have the following study issues concerning the radiation hardness of CCD sensors:

- effect of readout speed;
- how to inject the "fat zero charge";
- radiation damage effect on the spatial resolution;
- radiation damage by high energy ($>$ 10 MeV) electrons.

<u>Fast readout electronics</u> **: for improvement of radiation hardness and reduction of readout channel to 1300 ch**

Faster readout speed has advantages of less CTI increase by radiation damage and less number of readout channels in a limited readout time (6.7 msec) of JLC. Recently CCD signal processor (CSP) chips became commercially available at very low cost for digi-cam use. These chips have a correlated double sampler, a variable gain amp, and an ADC within a very small chip size (< 1cm^2). The readout and digitizing speed of these chips reaches 40 MHz. We are developing a CCD readout system using a CSP chip.