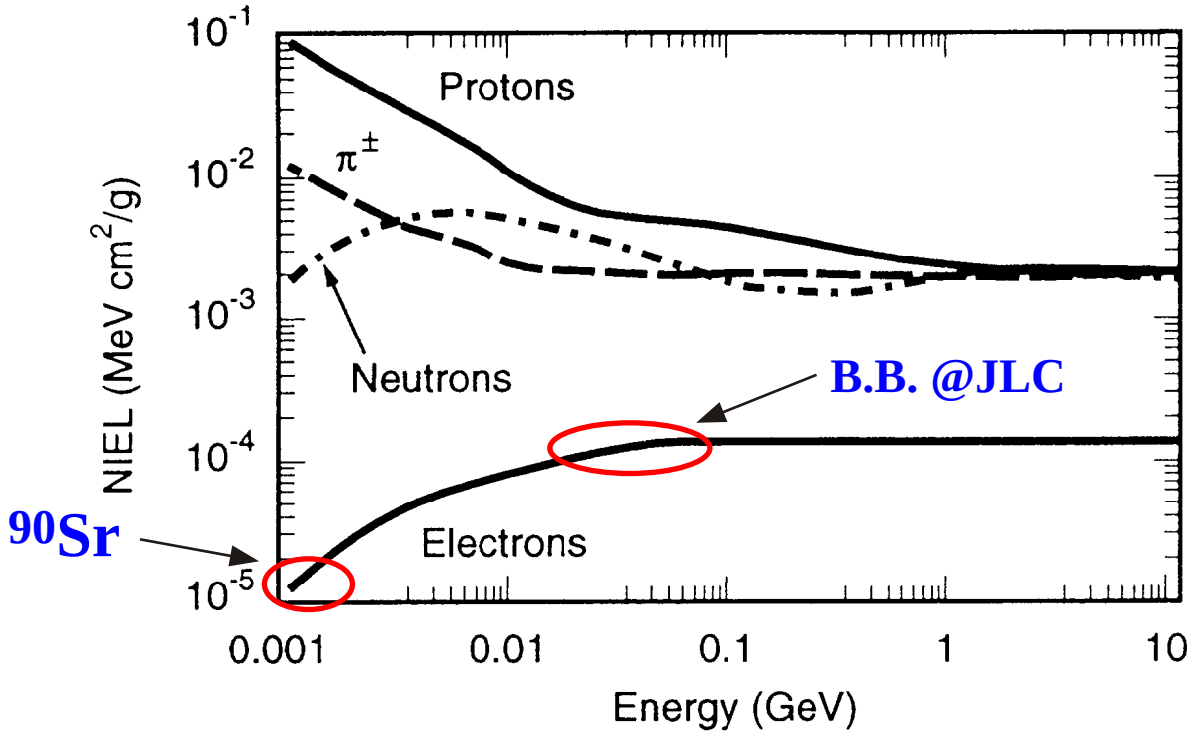
R&D Plan for CCD Vertex Detector in FY2002

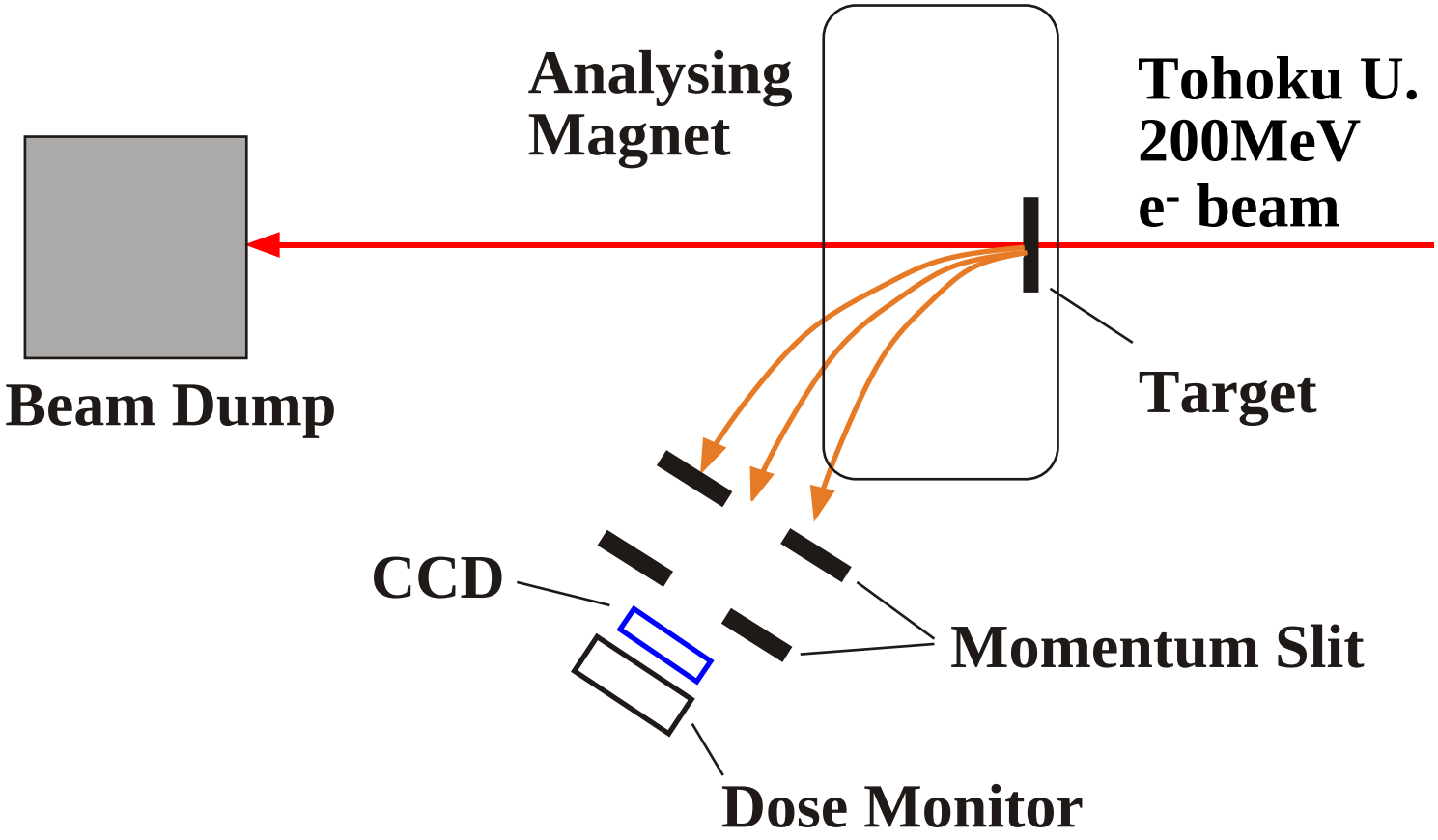
2002. 4. 12.
Y. Sugimoto

- Radiation Hardness (Niigata, KEK, Tohoku)
- New Readout Electronics (Niigata, REPIC, KEK)
- Thin Wafer (KEK)
- Simulation (Toyama, Niigata)
- New CCD (?)

Study of Radiation Hardness of CCDs against High Energy Electrons

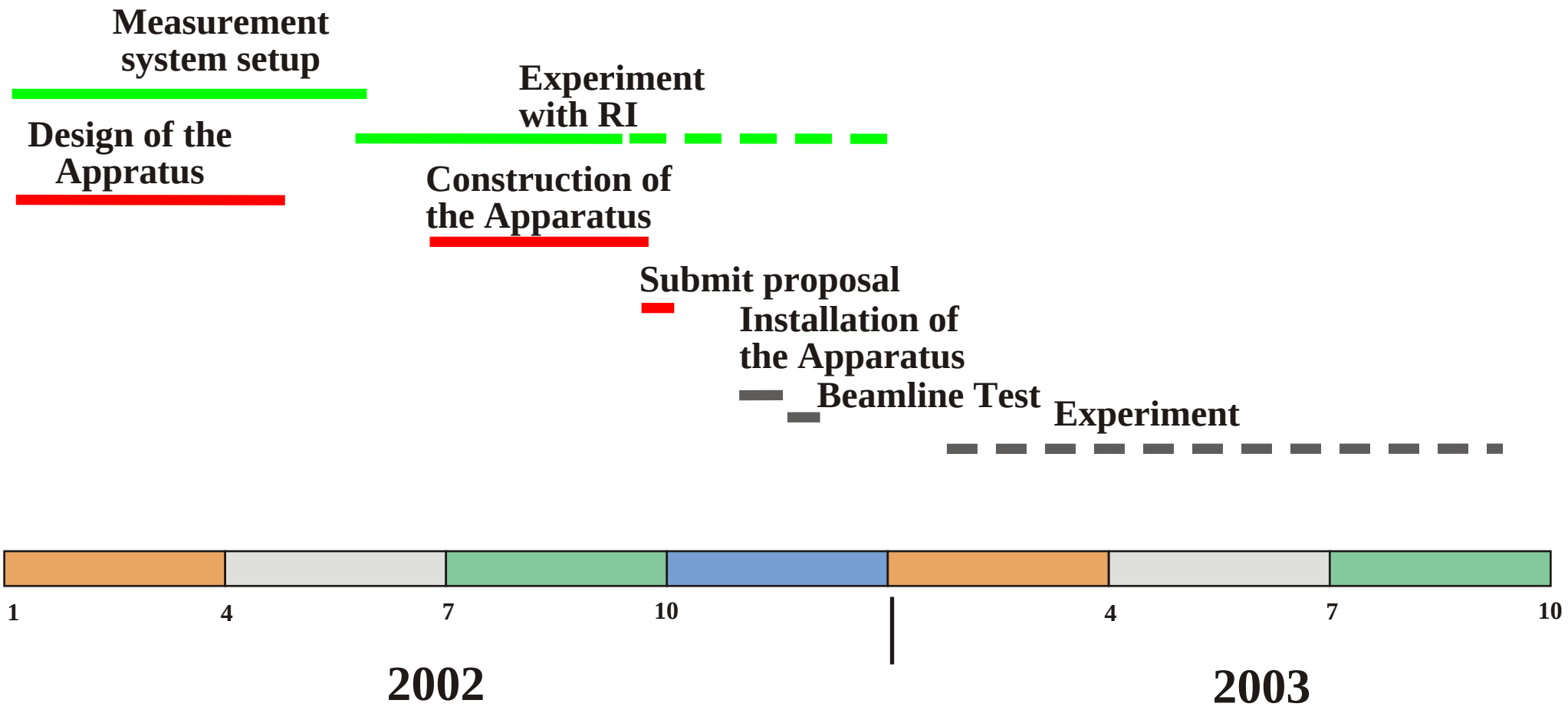


Apparatus



expose 10^{9}~10^{12}/cm^{2}

Schedule


Measurement system setup
Design of the Appratus
Experiment with RI
Construction of the Apparatus
Submit proposal
Installation of the Apparatus
Beamline Test
Experiment
1
4
7
10
4
7
10
2002
2003

New Readout Electronics

Targets & Motivation

1) Faster Readout Speed (>10MHz):

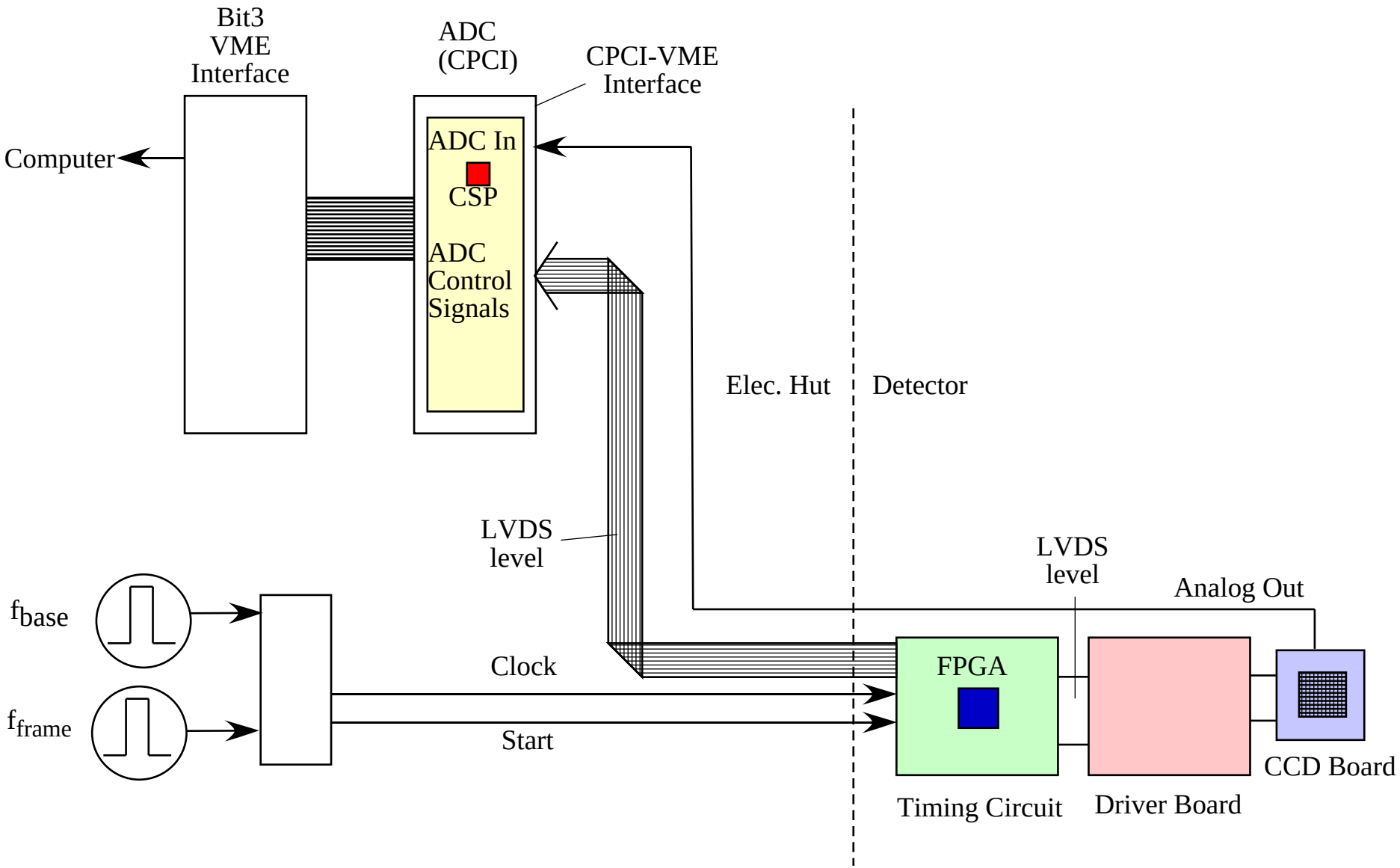
- to reduce number of readout channels at JLC
- to reduce effect of radiation damage (CTI) in horizontal register

2) Evaluation of CCD Signal Processor Chip:

- compact, low-power, and inexpensive IC including frontend electronics and 12bit/20MHz or 10bit/40MHz ADC

3) Digitization on Detector:

- to reduce number of cables -> reduce holes of detector
- high speed and low noise



New Readout Electronic : Step 1

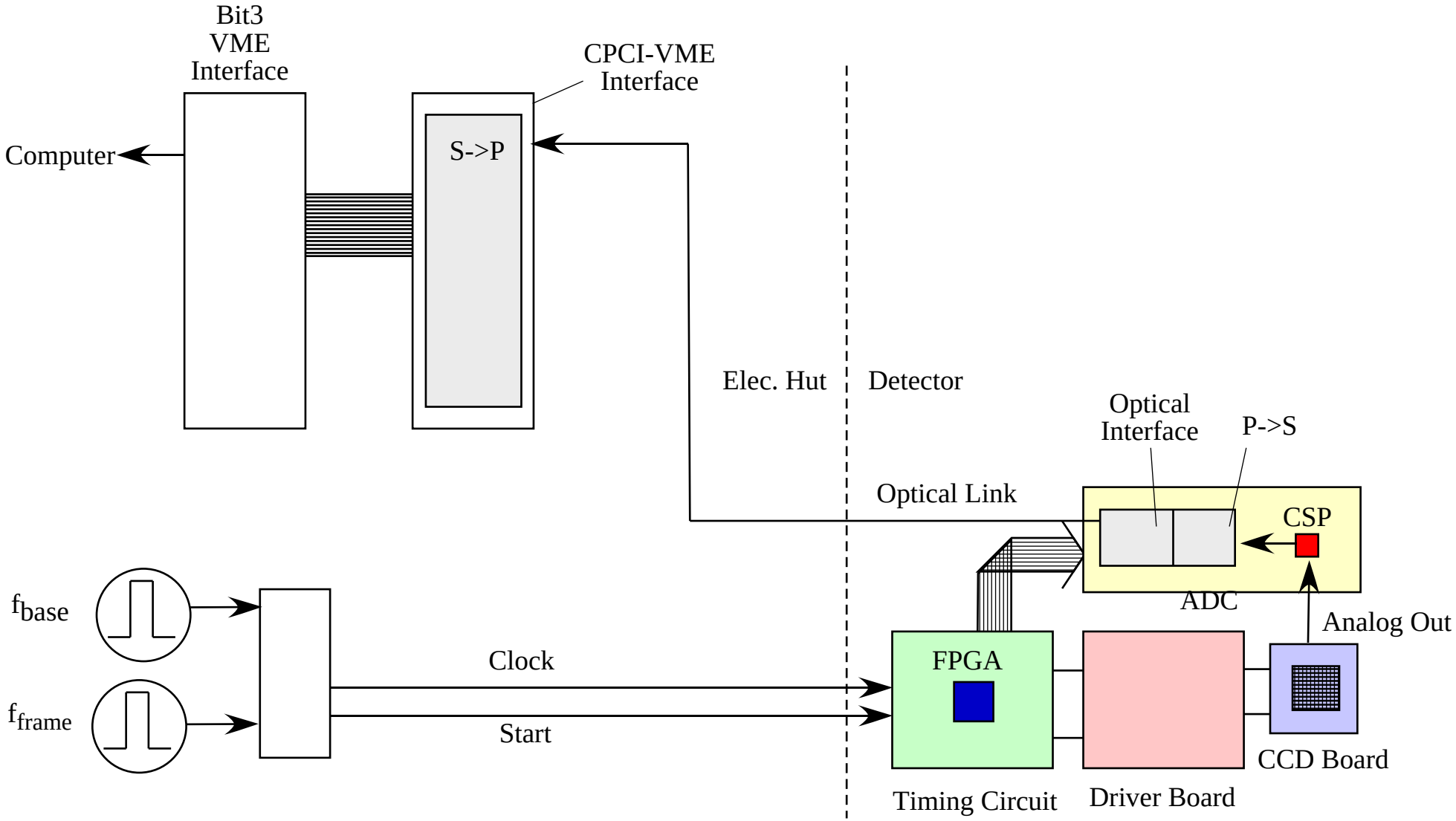
Spec. of the Chips

CCD Signal Processor : AD9840A / AD9844A

- 10 bit / 40 MHz or 12 bit / 20 MHz ADC
- 155 mW / 65 mW Power Dissipation
- Correlated Double Sampler
- 0 dB to 46 dB Variable Analog Gain
- Auxiliary Inputs for AC signal and Composit Video Signal
- 7 mm x 7 mm Chip Size (9 mm x 9 mm including lead pins)
- about $6 / chip

FPGA : XILINX VIRTEX-E Series

- 100 ~ 800 I/O
- 1.8 V Core Voltage
- Selectable I/O Level
- 622 Mbps Max.



New Readout Electronic : Step 2

Schedule

1) Fabrication of CSP evaluation board	~Jan. 2002
2) Test of CSP chips	Jan.~Mar. 2002
3) Design of Timing Circuit & ADC module	~Summer 2002 (?)
4) Fabrication of T.C. and ADC	~Winter 2002/3
5) Step 2	FY. 2003 (?)

New CCD

Impact Ionization