Electron and Neutron Radiation Damage Effects on a Two-Phase CCD

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Abstract

Ionization and bulk radiation damage effects in a two-phase CCD, operated in a Multi Pinned Phase (MPP) mode have been evaluated. Two-phase CCD's are one of the candidates for application in the vertex detector of a future linear collider. Flat-band voltage shifts, dark current, dark current spikes and charge transfer efficiency (CTE) were studied on devices, subjected to irradiation with fluencies reaching 4.3×10^{12} electrons/cm^2 and 8.9×10^9 neutrons/cm^2.

An additional source of dark signal in electron irradiated devices was observed and explained by impact ionization by holes, released by tunneling from defect states near the Si-SiO_2 interface. A model for the CTE in a two-phase CCD as a function of temperature, background charges and clock timing is described. Calculations based on the model are in a good agreement with the experimentally determined values of CTE in electron and neutron irradiated CCD's.

Keywords

CCD, Radiation Damage, Charge Transfer Efficiency.

I. Introduction

IN MODERN scientific experiments charge-coupled devices are finding extensive application as imagers and particle detectors. In high energy physics they are successfully used as vertex detectors for precise measurement of particle trajectories close to the interaction point [1]. Because of their high resolution and two-dimensional readout, CCD's are also the primary candidate for the vertex detector at a future e^+e^- linear collider. In the near vicinity of the collision point detectors face considerable radiation levels and the radiation damage effects become one of the important issues to be investigated. During their proposed 10-year service the CCD's will be exposed to fast particle irradiation with estimated fluencies equivalent to 5×10^{12} electrons/cm^2 and 5×10^9 neutrons/cm^2.

In the radiation environment of a linear collider we can expect both ionization and bulk damage effects to be present. Ionization damage effects are caused by trapped charge in the gate insulator, which leads to shift in the operating voltages [2] and increased density of defect states at the Si-SiO_2 interface. Energetic particles produce bulk damage by displacing silicon atoms from their lattice positions, thus creating defects in the band gap. Neutrons are known to produce regions of localized damage, resulting in an increased number of pixels with high dark current generation. These dark current spikes are a potential source of fake signals and although the expected neutron background is low, its influence should not be neglected.

Charge transfer efficiency (CTE) of buried channel CCD's is usually degraded by the presence of bulk defects. It has been shown [3]-[8], that CTE is sensitive to temperature, type of the defects, size of the signal packet, presence of background charge and timing of the transfer. To minimize charge losses during transfer a proper operating temperature should be selected, which usually lies below 200K [4], [9]. In a modern vertex detector it is desirable to operate the CCD's at near-room temperature to

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decrease its mechanical instability caused by the cooling, as well as to reduce the material between the interaction point and outer detectors [10].

At near-room temperatures the dark current of the CCD may deteriorate the signal to noise ratio and the overall performance of the detector. Devices using Multi Pinned Phase (MPP) mode [11], [12], feature reduced dark current and can be attractive in such applications. In MPP mode the Si-SiO_2 interface of a buried channel CCD is biased into inversion and populated with holes, leading to suppression of the carrier generation from interface defect states. Additionally, this method has the ability to reduce the dark current from the interface states formed during irradiation and can offer an increased radiation hardness [12]. Recently, the parameters of MPP CCD's as track detectors have been investigated and they have shown good performance as minimum ionizing particles (MIPs) detectors at temperatures as high as +5°C [13].

From the results of previous works [4], [5], [9], we can expect that a buried channel CCD, subjected to radiation damage will exhibit an imperfect CTE at near-room temperature due to presence of bulk traps. Therefore, for a heavily damaged CCD some methods for CTE improvement have to be employed, for example using background charge ("fat zero") [8]. This requires a detailed study of the CTE as a function of temperature and clock timing, taking into account the presence of the dark current and the background charge.

In this work we study the flat-band voltage shifts, the dark current, the dark current spikes ("hot pixels") and the charge transfer inefficiency (CTI), defined as (1−CTE), of a two-phase CCD. In Section II we describe the experimental setup and in Section III the results on ionization damage effects and dark current. In Section IV a model for the CTI in a two-phase CCD is given. In Section V the experimental results and discussion on CTI are presented, followed by a conclusion in Section VI.

II. Experiment

The experiments were carried out on Hamamatsu Photonics S5466 CCD's, which are commercially available and do not employ any "radiation hard" fabrication technology. The devices are two-phase, full-frame transfer, buried channel type with a 10μm epitaxial layer. They have 512×512 active pixels with size 24μm×24μm. In MPP mode the positive and the negative amplitudes of the clock pulses, recommended by the manufacturer are $V_{cc} = 6V$ and $V_{ee} = -8V$. The devices were used at their maximum readout speed of 250 kpixels/second. The CCD's were read out every 3 seconds using a 12-bit ADC; and the time to collect one frame, including the non-imaging pixels and the overclocks, was about 1.3s.

During the electron irradiation the devices were exposed to a 9.7mCi ^{90}Sr source at room temperature. Two of the CCD's were unbiased and one device was clocked during irradiation. The irradiation rate was estimated to be 1.4×10^{10} cm^{-2}h^{-1} from geometrical considerations. A calculation of the dose rate was carried out by measuring the average current in the reset drain node of the CCD. That current under continuous readout conditions was 3.1±0.2 nA. Using a value of 3.6eV for the ionization energy in silicon, the dose rate was calculated to be 1080±65 rad per hour.

For the neutron irradiation an Amersham ^{252}Cf source with an emission of 4.6×10^5 neutrons/s was used. Under the same geometrical conditions as of the electron irradiation, the neutron fluence was estimated to be 1.5×10^7 cm^{-2}h^{-1}. The pins of the CCD were kept grounded for the reasons explained later in the text.

Several hours after irradiation the CCD's were cooled down in a vacuum cryostat to −26°C and the shift of the operating voltage needed to achieve MPP mode was measured. If a correction was necessary, the negative drive pulse voltage of the vertical (parallel) register V_{ee}^{V} was changed by the corresponding value. We kept the operating voltage of the horizontal (serial) register V_{ee}^{H} unchanged, because its dark current was usually two orders of magnitude lower than that of the vertical register due to its faster readout. To avoid unwanted charge generation and injection from the input structures

of the registers, the input gates were also biased to V_{ee}^{V} and V_{ee}^{H}, correspondingly.

For the CTI measurements we used charge packets of 1620 electrons, created by the 5.9keV Mn-K_α line of a 24μCi ^{55}Fe source. Operating the devices in MPP mode, we measured the CTI of their vertical and horizontal registers over the temperature range from -100 to $+20$°C. After sufficient averaging, the dark signal of each pixel was stored into memory and the calculated in this way dark frame was then subtracted pixel by pixel during the X-ray illumination. We used only isolated-pixel events: i.e. around any pixel having signal above the selectable threshold we imposed the condition that its neighbouring pixels not contain charge greater that 3 times the normal deviation of the dark current σ_{dark}. By averaging the signal from pixels which contained charge within the window of the ^{55}Fe peak over the horizontal rows and vertical columns, we were able to measure the vertical and horizontal CTI with accuracy of better than 10^{-5} for non-irradiated devices. The density of the isolated X-ray events was not more than 1 X-ray per 440 pixels. The dark current was also measured over the same temperature range. A miniature Pt resistor was attached to each CCD for better temperature monitoring.

III. Results on Ionization Damage Effects and Dark Current

A. Shift in the MPP Threshold Voltage

For a CCD with a MPP mode capability a convenient method for measuring the flat-band voltage shift is to observe the voltage needed to invert the Si-SiO_2 interface. Since that voltage is negative referred to the substrate, after build-up of positive charge in the oxide, the applied voltage should increase in absolute value. For *n*-channel CCD's the electric field in the oxide is pointed toward the gates, holes are trapped mostly at the gate-SiO_2 interface and they have less impact on the MPP threshold voltage if they were trapped at the Si-SiO_2 interface. The shift of the threshold voltage V_{ee}^{MPP} for a device irradiated with its pins grounded is shown on Fig. 1.

It can be noticed that after irradiation to 1.7×10^{12} e^-/cm^2 the transition into MPP mode is not abrupt. This behaviour can be explained by non-uniformity of irradiation and the flat-band voltage shifts, which leads to spread in the threshold V_{ee}^{MPP} in pixels at different distance from the center of the CCD.

One of the devices was irradiated to 4.3×10^{12} e^-/cm^2 and its V_{ee}^{MPP} threshold was well above 11V, which exceeded the safe limit of the MOS drivers. The swing of the clock pulses in our experiments is limited by the maximum supply voltage of the MOS drivers to $(V_{cc} - V_{ee}) < 18V$. This sets a limit to the flat-band voltage shift that can be accommodated by adjusting the amplitude of the clock pulses.

For a device clocked under irradiation we observed significantly higher change in V_{ee}^{MPP}, corresponding to higher flat-band voltage shift (Fig. 2). Our result is consistent with the works of Robbins et al [9] and Hopkinson [14], showing that zero bias during irradiation produces the smallest flat-band voltage shift.

In the neutron irradiated CCD no significant flat-band voltage shift was observed (Fig. 3). Because of the minor ionization damage, no bias dependence of the flat-band voltage shift was expected and the device was irradiated unpowered.

B. Interface States and Dark Current

At a value of $V_{ee}^{V} < V_{ee}^{MPP}$, the Si-$SiO_2$ interface is partially depleted and the dark current generation is dominated by the interface states in both non-irradiated and irradiated devices. Electron irradiation introduces defects in the interface, which increase the dark current when the device is not in MPP mode. At a value of $V_{ee}^{V} > V_{ee}^{MPP}$, the Si-$SiO_2$ interface is populated by holes and the CCD demonstrates effective suppression of the surface component of the dark current by almost 4 orders of magnitude (Figs. 1, 2). In that condition the dark current is limited by carrier generation in the bulk silicon, indicating that bulk damage is also present.

The dark current in MPP mode in both electron and neutron irradiated devices increased after irradiation due to creation of bulk traps. In the neutron irradiated CCD the bulk damage was dominant (Fig. 3). Newly formed interface states due to the gamma background of the neutron source are difficult to observe, because their contribution to the dark current is smaller than the increase of the bulk generation. The dark current of an electron irradiated CCD in normal and MPP mode is given on Fig. 4. The ability of the MPP mode to suppress the surface component of the dark current and to extend the operating temperature range of the CCD is clearly demonstrated. Fresh CCD's showed a temperature dependence of the bulk dark current of $\exp(-0.57\mathrm{eV/kT})$, which did not change significantly after receiving a fluence of 1.7×10^{12} electrons/cm^2 or 8.9×10^9 neutrons/cm^2.

A reverse annealing of the interface state density was observed after storage of devices unpowered at room temperature (Fig. 2). This commonly observed effect is explained by slow buildup of interface states [14].

C. Additional Source of Dark Current

In the electron irradiated CCD's we observed another component of the dark current, which was superimposed on the bulk current. This spurious current, which can be called "dark current pedestal" (DCP) is not related to the accumulation time of the readout cycle [15] and is produced by the clocking. The DCP provides background charge in the CCD and decreases the measured CTI through the "fat zero" effect, as will be shown in Section V. In this work we present a detailed investigation on the DCP and a possible explanation.

In fresh CCD's we noticed presence of spurious dark signal, which appeared at high amplitude of the clock pulses. It had a maximum value of 40 e$^-$ at $V_{ee}^V = 11$V in one of the samples. This current is similar to the spurious dark signal observed in virtual-phase CCD's utilizing surface pinning for reduced dark current generation. Hynecek [16] explains that current by impact ionization by holes returning to the channel stops and to the adjacent gates after the surface potential has been switched from inversion to depletion. In his model the spurious current is generated on each clock and is essentially independent on the width of the clock pulses.

After electron irradiation we observed large increase of the DCP in devices operated in MPP mode, while such a current was not present in the same CCD's clocked in normal mode, in which the surface is not inverted. DCP was not observed also in the neutron irradiated device.

The temperature dependence of the DCP is shown on Fig. 5. It can be seen, that at low temperature the DCP can be several orders of magnitude higher than the bulk current, which is plotted on Fig. 4. The spurious dark current depends on the readout speed of the CCD through the width of the shift pulse of the vertical register. On Fig. 6 this dependence is plotted with the temperature serving as a parameter. At low temperature the dependence on the clock width is very close to exponential emission with time constant of approximately 10μs. The dark current pedestal exhibits also a voltage dependence on the amplitudes of the clock pulses of the vertical register. The dependencies on the values of V_{ee} and V_{cc} are shown on Fig. 7(a) and Fig. 7(b), respectively.

In the horizontal register the video level of the overclocked pixels, which is used as a reference, is sensitive to the amplitude of the clock pulses and to the temperature due to capacitive feedthrough to the output node. After electron irradiation this dependence became much stronger, and it was impossible to observe analogous spurious signal in the horizontal register.

Since in electron irradiated CCD's there is significant creation of defects in the Si-SiO_2 interface, a conclusion can be drawn that the increase of the DCP is due to the newly formed interface states. The dependence of the DCP on the width of the shift pulse and on the temperature suggests that another mechanism beside impact ionization is involved. Therefore an extension of the model proposed by Hynecek is needed to explain our experimental results.

In the low-temperature part on Fig. 5 the DCP decreases with the temperature, because the ionization rate is lower at higher temperatures [17]. Hence, the process that supplies holes for acceleration

should have weak or no temperature dependence. Because the DCP is a function of the width of the shift pulse, there must be additional holes taking part in the impact ionization, beside those quickly returning to the channel stops. We suggest that in this temperature region holes are released by tunneling from near-interface defect states.

Tunneling emission and injection of electrons into defects in the oxide, situated near the Si-SiO_2 interface has been observed previously [18], and it has been shown to be a temperature independent process. In the case of S5466 CCD holes are injected during inversion and then emitted by tunneling from near-interface traps in the regions between the gates, where the electric field can be higher than 10^5 V/cm. After emission, holes are accelerated by the electric field and create electron-hole pairs by impact ionization. Electrons are collected as DCP signal, as shown on Fig. 8. The effect occurs every time one of the phases is held at V_{ee} and the other one at V_{cc} and is therefore proportional to the number of transfers. In the high-temperature region in Fig. 5 holes are emitted by thermal ionization from interface states, which has an exponential temperature dependence and we observe increase of the DCP with temperature.

This model qualitatively explains the observed characteristics of the DCP and its high value at low temperature. However, due to the complex structure of the CCD, quantitative model describing DCP would require measurements on simpler devices, such as test MOS capacitors in the CCD chip, which are not available at present.

D. Hot Pixels

Hot pixels are time-varying fluctuations of the dark current [19], that can produce false signals when the CCD is used as a vertex detector. Increase of the number of hot pixels in a virtual-phase CCD, irradiated with fast protons or neutrons have been observed previously [12], [20]. Their presence has been explained by the high electric fields in the devices and the radiation damage effects. In a 2-phase CCD high internal electric fields are also present, and we can expect effects similar to those observed in virtual-phase CCD's.

Fresh and electron irradiated devices did not have dark current spikes even at relatively high temperature (Fig.9(a)-9(d)). In the neutron irradiated CCD however, we observed significant creation of hot pixels (Fig.9(e)) after irradiation with a fluence as low as 2.4×10^8 n/cm^2. After subtraction of the dark frame on a pixel by pixel basis, the resulting distribution (Fig.9(f)) is close to that of a electron irradiated CCD. This is an indication that the current generation in the hot pixels is not random and it has a linear time dependence. Therefore, the influence of the dark current spikes can be suppressed significantly by subtracting individually the average dark current of each pixel.

Because some of them contain quite high charge, the temperature range of the measurements is limited by the input range of the ADC. At lower temperatures the number of dark current spikes steeply diminishes. The amplitude of the hot pixels would decrease also if the CCD was read out faster, which we were not able to confirm due to the device limitations. We think that at higher readout speeds or at temperatures lower than 0°C (using slow readout) hot pixels will not impose any limitation to the application of the S5466 CCD in the expected neutron environment.

IV. Charge Transfer Model

A. Theory of Charge Trapping

In a buried channel CCD charge is transported far from the defect states in the Si-SiO_2 interface and only the interaction of the signal packets with the bulk traps can be considered. In the presence of bulk defects electrons can be trapped with a capture time constant of τ_c and consequently released with an emission time constant of τ_e. For a defect at energy position E_t below the conduction band the Shockley-Read-Hall theory gives

$$\tau_e = \frac{1}{\sigma_n X_n v_{th} N_c} \exp\left(\frac{E_t}{kT}\right) \tag{1}$$

and

$$\tau_c = \frac{1}{\sigma_n v_{th} n_s}, \tag{2}$$

where

σ_n = electron capture cross section,
X_n = entropy change factor by electron emission,
v_{th} = thermal velocity for electrons,
N_c = density of states in the conduction band,
k = Boltzmann's constant,
T = absolute temperature,
n_s = density of signal charge.

Charge losses occur when defects capture electrons and emit them at a later moment, so that the released charge cannot join the original signal packet from which it has been trapped. Since the charge is transferred within several nanoseconds to the next pixel by the fringing fields, the trapping during the transfer time can be neglected. We consider effects of trapping and emission solely during the charge dwell time. There are several commonly observed defects in electron or neutron irradiated n-type silicon [21], [22]. For near-room temperature application we can consider only defects that are known to cause noticeable CTI in that temperature range [4], [5], [9]. Such traps are the phosphorous-vacancy ($P-V$) center and the single charge state of the divacancy ($V-V^-$). Another defect at E_c−0.30eV with an unknown nature has also been observed [5], [6], with a creation rate several times smaller than that of the $V-V^-$ and $P-V$ centers. Table 1 gives the parameters of the three traps, which are within the values found in the literature data. Following the approach of A. Holland [5], the charge storage volume was estimated to be 24μm×6μm×0.15μm. This volume is considered constant for charge packets smaller than few thousand electrons.

TABLE I
PARAMETERS OF THREE TRAPS OF INTEREST.

Defect	$E_c - E_t$, eV	σ_n, cm^2	Reference
$P-V$	0.42	3×10^{-15}	[5]-[8], [21], [22]
$V-V^-$	0.39	4×10^{-15}	[6], [21], [22]
unknown	0.30	5×10^{-15}	[5], [6]

B. CTI Model for the Horizontal Register

In the horizontal register charge is transferred by applying square wave pulses, shifted by 180°, to the gates P1 and P2 (Fig. 10). Because the S5466 CCD utilizes a p-type implant to form the potential barriers for charge separation within one pixel, the electrons are stored in the potential wells under the part of the gate structure next to the implant. We apply the Shockley-Read-Hall theory to the potential well in the storage region under the phase P1. We consider the case of a charge packet transported along the horizontal register at a distance of m pixels from the previous signal packet. The CTI is studied by calculating the ratio of filled traps, defined as $r_f = n_f/N_t$, where n_f is the concentration of the defects, that have captured an electron, and N_t is the total defect concentration. Let us suppose that at the moment A the traps in the region have an occupancy of r_f^A. After the voltages applied to P1 and P2 reverse their values, the defects start to emit their trapped charge and at the moment B the ratio of filled traps becomes

$$r_f^B = r_f^A \exp(-t_w^H/\tau_e), \tag{3}$$

where t_w^H is the width of the horizontal shift pulse. When the signal packet arrives to the region, the concentration of filled traps n_f under P1 and the occupancy r_f^C at the moment C can be found by solving the equation

$$\frac{dn_f}{dt} = \frac{N_t - n_f}{\tau_c} - \frac{n_f}{\tau_e}, \tag{4}$$

with an initial condition of $n_f/N_t = r_f^B$, and τ_c determined from the concentration of signal charge n_s (2). Provided that $n_s \gg N_t$, the solution is

$$r_f^C = \left(r_f^B - \frac{\tau_e}{\tau_e + \tau_c}\right) \exp\ \left\{-t_w^H \left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)\right\} + \ \frac{\tau_e}{\tau_e + \tau_c}. \tag{5}$$

This result holds for the general case where full occupation of the traps in the presence of signal charge is not assumed. For very low values of n_s however, τ_c becomes a function of the trap occupation and cannot be considered a constant. This usually corresponds to the case of transporting very small charge or the dark current alone. In that condition (5) is no longer valid and r_f^C is obtained by solving the equation (4) numerically.

After the charge has been shifted to the region under P2, at the moment D the ratio of filled traps becomes

$$r_f^D = r_f^C \exp(-t_w^H/\tau_e). \tag{6}$$

The charge loss in the region under P1 is proportional to the difference between r_f^D and r_f^B. Because the phases P1 and P2 are equivalent, the horizontal CTI per pixel is given by

$$HCTI = 2\frac{N_t}{n_s}(r_f^D - r_f^B). \tag{7}$$

The occupancy r_f^A can be found by applying (3)-(5) m times, starting with an initial condition of r_f^A = 1, and using n_s=n_{dark}. The initial condition follows from the assumption, that the signal charge usually contains large number of electrons, which can fully occupy all the traps in the storage area. In this way we can simulate the effect of the density of the X-ray events on the CTI. It is also possible to investigate the effect of the background charge on the CTI by varying the value of n_{dark}.

C. CTI Model for the Vertical Register

The charge transfer in the vertical register has to be considered separately for the regions under P1 and P2 because of the different time the charge packet spends under the two halves of the pixel. The clock sequence used for the charge transfer and the diagram of the consecutive transfer stages are given on Fig. 11. Charge is stored entirely under P2 during the horizontal shift time, which affects to a great extent the CTI caused by that region.

For the well under P1 two transfer steps have to be considered: (a) transfer of charge from the previous pixel (A-B); and (b) charge transfer to P2 of the same pixel and emission of trapped electrons (B-C). The filling ratios are obtained from (3) and (5) using t_w^V for the width of the shift pulse. Supposing that the initial trap occupation under P1 is r_f^A(P1), the CTI for that region is

$$CTI(P1) = \frac{N_t}{n_s}(r_f^C(P1) - r_f^A(P1)). \tag{8}$$

There are 3 transfer steps for the region under P2: (a) electron emission (A-B); (b) the charge transferred from P1 stays under P2 for the period of t_w^V plus the horizontal shift time (B-C-D); and (c) charge transfer to the next pixel and emission of trapped electrons (D-E). For the region under P2 the CTI is

$$CTI(P2) = \frac{N_t}{n_s}(r_f^E(P2) - r_f^B(P2)). \tag{9}$$

The filling ratios for the steps (a) and (c) are obtained from (3) using t_w^V for the width of the shift pulse. For the step (b) the filling ratio is calculated from (5) using for the width of the shift pulse the value $t_w^V + 2{\times}t_w^H{\times}hpix$, where $hpix$ is the number of pixels in the horizontal register. The CTI per pixel of the vertical register is then given by

$$VCTI = CTI(P1) + CTI(P2). \tag{10}$$

The initial occupancies r_f^A(P1) and r_f^A(P2) can be found in the same way as those used for the horizontal register.

It is important to study the dependence of the CTI on the concentration of background and signal charges, because it affects significantly the experimentally determined CTI values [8]. For near-room temperature operation the dark current, which has an exponential temperature dependence, should be considered even for MPP devices. Additional source of background charge can be the dark current pedestal, described in section III.C, or an artificially introduced charge through the input structure of the CCD. In a vertex detector a MIP produces about 1080 electrons in a 10μm thick epitaxial Si layer [13], so that we can assume that the charge created in each pixel contains approximately the same number of electrons. Under these considerations, we study only the dependence of CTI on the background charge; and to be able to compare with the experimental data the signal charge is taken to be 1620 electrons.

On Fig. 12 the modeled HCTI and VCTI are plotted as a function of the temperature and the number of the "fat zero" electrons for the $V-V^-$ center with parameters listed in Table 1. The values of $X_n = 2$ and $v_{th}N_c = 1.6{\times}10^{21}T^2$ cm^{-2}s^{-1} were used in the calculation. The widths of the vertical and the horizontal shift pulses are typical to the values used in the experiment. Fig. 12 shows that even small background charge can decrease significantly the CTI. The peak of the VCTI occurs at lower temperature than the peak of the HCTI because $t_w^V > t_w^H$. It is seen that a significant reduction of the HCTI can be achieved in the temperature range from -40 to $+20$°C by introducing "fat zero" charge. The VCTI also decreases in the presence of background charge, but the effect is relatively smaller than that on the HCTI. Due to the different time the charge spends in the regions under P1 and P2 of the pixels in the vertical register, the behaviour of the VCTI as a function of the background charge differs from that of the HCTI.

The simulation on Fig.13 shows that the region under P1 is the main source of VCTI in the presence of background charge. The model shows, that the reason for this behaviour is that the traps in the region under P1 have enough time to become empty during the horizontal shift time. When the signal packet arrives to P1, trap occupation is low and almost all of them can capture electrons. The signal comes under P2 shortly after the dark charge has left the region, trap occupation is still high and less electrons can be captured. From Fig. 13 it is seen that the CTI caused by region under P1 is less sensitive to the presence of background charge than the region under P2. Because of this feature, introducing "fat zero" charge has smaller effect on the VCTI, than on the HCTI.

V. Results on CTI and Discussion

The results from the CTI measurements on electron irradiated S5466 CCD's, together with modeled results are shown on Fig. 14(a). Constant voltage swing of the vertical shift pulse ($V_{cc} - V_{ee}$) = 14V was kept throughout the measurements even if the value of V_{ee} had to be adjusted to operate the CCD in MPP mode. This was done in order to compensate for the flat-band voltage shift. Modeling was performed using the experimental values of the dark current on Fig. 4 and of the DCP on Fig. 14(b). The pre-irradiation VCTI is reasonably explained by the presence of a defect at $E_c{-}0.44$eV with $\sigma_n = 3{\times}10^{-15}$ and a concentration of $9{\times}10^9$cm^{-3}. Horizontal CTI before irradiation was below the measurable limit of 10^{-5}.

The modeling on electron irradiated CCD's showed that a trap at $E_c{-}0.37$eV with $\sigma_n = 4{\times}10^{-15}$ cm^2 was responsible for the observed increase of the VCTI. The simulated results on Fig. 14(a) are

based on the presence of the two traps at $E_c-0.37$eV and $E_c-0.44$eV. The concentration of the trap at $E_c-0.44$eV, derived from the model increases unsignificantly under irradiation. The introduction rate of the defect at $E_c-0.37$eV is very close to linear function of the electron fluence and it is calculated to be about 0.16 cm^{-1}. The CTI of the horizontal register is less than 10^{-4} in the whole temperature range after irradiation. This result can be easily explained by the HCTI dependence on the background charge shown on Fig. 12. The peak in the HCTI, which would have occurred at high temperature is suppressed by the dark current pedestal and the exponentially increasing dark current.

In the modeling it is difficult to separate the effects of the defect energy and its capture cross section, and exact identification of the trap at $E_c-0.37$eV is not straightforward. Because of the high electric fields present in the S5466 CCD, the assumed trap energy may be reduced by the Frenkel-Poole field enhanced emission. In the region where the gates P1 and P2 overlap the electric field has its maximum when one of the electrodes is held at V_{cc} and the other one is at V_{ee}. Assuming 1μm for the width of the high field region, the maximum energy reduction is $(e\mathcal{E}/\pi\epsilon_{Si})^{1/2} = 0.082$ eV, where $\mathcal{E}$ is the field intensity. Taking 6μm for the width the charge storage region, the energy reduction averaged over a pixel is estimated to be 0.027eV. This calculation leads us to the conclusion, that the observed defect at $E_c-0.37$eV may be a center, which apparent energy position has been reduced by the Frenkel-Poole effect. This defect is possibly the $V-V^-$ center, or because the $V-V^-$ and $P-V$ traps are very difficult to resolve in our measurements, the peak in the VCTI spectra may be the combined effect of both.

The observed creation rate of 0.16 cm^{-1} for the defect at $E_c-0.37$eV after electron irradiation is in a contrast with the known value for the $V-V^-$ center of 0.015 cm^{-1} [4], [21]. Therefore, we are brought to the conclusion that it is more likely to be the $V-V^-$ center which introduction rate is higher than that of the $P-V$ complex [21].

On Fig. 15 the experimentally obtained values of the VCTI in a neutron irradiated CCD are plotted together with the simulated results. The HCTI was below 5×10^{-5} in the whole temperature range before and after irradiation to 8.9×10^9 neutrons/cm^2. The VCTI data of a fresh device is well described by the defect at $E_c-0.44$eV. After neutron irradiation, the fit of the model to the data showed that the same defect at $E_c-0.37$eV caused increase in the VCTI. The measured creation rate of that center is about ten times larger than that observed in the electron irradiated devices. This supports the suggestion of a $V-V^-$ center, because it is known to be produced more intensively by fast neutrons, than by electrons [3], [22]. The agreement of the model with the experiment is deteriorated at high temperatures, probably because the charge of the hot pixels reduces the measurable VCTI by the "fat zero" effect.

VI. Conclusion

In this work we have investigated the ionization and bulk radiation damage effects in a two-phase buried channel CCD. After electron irradiation from a beta source, significant flat-band voltage shift and large increase of the density of the interface states were observed, as well as creation of bulk traps. The shift of the MPP threshold voltage, which served as a measure of the flat-band voltage shift was higher in the device irradiated with applied clock, than in the unpowered device.

In the electron irradiated CCD's additional dark current was observed, which was associated with impact ionization by holes, accelerated to high velocities by the strong electric field between adjacent gates. At low temperatures holes are supposed to be provided by tunneling from defects near the Si-SiO_2 interface. Electrons created by the impact ionization are collected in the potential wells, providing "fat zero" effect and decreasing the measured CTI values. In the neutron irradiated device bulk damage was dominating. In this CCD we observed also creation of dark current spikes, which influence could be reduced by subtraction of the dark frame on a pixel by pixel basis.

A simple model for the charge transfer inefficiency is presented, which allows to predict the CTI as a function of the temperature, timing of the transfer and the the concentration of background charge.

The model is in a good agreement with the experimental results on electron and neutron irradiated CCD's. A defect at $E_c-0.37$eV appears in both electron and neutron irradiated devices. We have found that the combination of the observed pre-irradiation defect at $E_c-0.44$eV and the trap at $E_c-0.37$eV gives the best fit to the experimental VCTI data. Due to the high electric fields present in the CCD, we suggest that the trap at $E_c-0.37$eV is the $V-V^-$ center, which apparent anergy position has been reduced by the Frenkel-Poole effect. The concentration of bulk defects appears to be a linear function on the particle fluence. In the neutron irradiated CCD the introduction rate of the defect at $E_c-0.37$eV is about 10 times higher than that in the electron irradiated devices. The proposed model can be used for evaluation of CTI in two-phase CCD's over a wide range of operating conditions.

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