Radiation Damage Effects in CCD Sensors for Tracking Applications in High Energy Physics

Ph.D. Thesis

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Abstract

This thesis presents systematic studies on the radiation damage effects in 2- and 3-phase Charge Coupled Devices (CCD). CCDs are one of the primary options for tracking devices at the vertex detector of a future Linear Collider due to their high precision and two-dimensional resolution. The radiation backgrounds near the interaction point impose considerable challenge to the tolerance of the CCD sensors to radiation damage effects. To estimate the effects from the expected radiation background, surface and bulk damage have been extensively studied in electron- and neutron-irradiated CCDs from two different manufacturers, Hamamatsu Photonics and Marconi Applied Technologies.

Special attention was paid to the application of CCD in radiation environment at near-room temperatures. Multi Pinned Phase (MPP) mode CCDs, which offer more than an order of magnitude lower dark current than conventional devices were studied. The flat band voltage shifts, caused by ionizing radiation have been found to be considerable, especially in devices irradiated under bias. In Hamamatsu devices additional dark signal, induced by the clocking was observed and found to be a major device problem. That current is explained by impact ionization from holes, emitted from radiation-induced defects at the Si-SiO_2 interface.

Dark current spikes ("hot pixels"), some of which generate current in the form of Random Telegraph Signals (RTS) were found in neutron irradiated devices. It was shown, that although potentially dangerous, RTS are unlikely to be a limiting factor to the device application at sufficiently fast readout even at room temperatures.

Charge transfer losses, or Charge Transfer Inefficiency (CTI) in CCDs, caused by radiation-induced bulk defects was one of the major issues under study. Charge losses in 2- and 3-phase CCDs, which are nowadays the most widely used devices, were studied both theoretically and experimentally. The influence of the clock timing and pattern, temperature, dark current, signal density and pixel occupancy on the CTI was investigated in order to find the optimal operating conditions for reduced charge losses. The clock

frequency and the dark current are shown to have larger influence on the CTI of the serial register than on the vertical register because of the different clocking schemes in the two sections.

A modified clock pattern, which can decrease the vertical CTI in 2-phase CCDs by ≈ 1.8 times was developed and tested. It was shown, that the most effective method for minimizing charge losses is filling the traps by an additionally injected charge ("fat zero") in the device. A new method for thermal generation of fat zero effect in MPP CCDs is proposed, which offers several advantages and can be applied at near-room temperature on a variety of devices.

The results on radiation-induced CTI contribute to the further understanding of the problem and offer solutions for minimizing the effects of bulk traps on the performance of the CCDs. The results of this study can be used for building better, radiation-resistant CCDs and to optimize their operating conditions for reducing the influence of radiation defects on the device characteristics.

Contents

1 CCD Vertex Detector **1**

1.1 Vertex Detectors in High Energy Physics 1

1.2 CCD Principles and Operation 3

1.2.1 Introduction to CCDs 3

1.2.2 Buried Channel CCD 5

1.2.3 Multi Pinned Phase CCD 5

1.2.4 CCDs as Particle Detectors 6

1.3 CCD–based Vertex Detector 8

2 Radiation Damage Effects in CCDs **11**

2.1 Surface Damage 12

2.1.1 Radiation-Induced Trapped Positive Charge 12

2.1.2 Radiation-Induced Interface Traps 14

2.2 Bulk damage 15

2.2.1 Basic Mechanisms and Defects 15

2.2.2 Dark Current and Charge Transfer Losses 19

3 Experimental Results on Irradiated CCDs **23**

3.1 Experimental Setup and Measurement Techniques 23

3.1.1 Investigated CCDs 23

3.1.2 Experimental Setup 24

3.1.3 CTI Measurement 28

3.1.4 Dark Current Measurement 29

3.1.5 CCD Irradiation 29

3.2 Ionization Damage Effects and Dark Current 30

3.2.1 Flat Band Voltage Shifts 30

3.2.2 Interface and Bulk Dark Current . . . 34
3.2.3 Spurious Dark Current . . . 36
3.2.4 Hot Pixels . . . 41

4 Charge Transfer Model and CTI Measurements 51
4.1 Theory of Charge Trapping . . . 51
4.2 Charge Transfer Model for 2-phase CCD . . . 53
4.2.1 CTI Model for the Horizontal Register . . . 53
4.2.2 CTI Model for the Vertical Register . . . 55
4.3 Charge Transfer Model for 3-phase CCD . . . 60
4.3.1 CTI Model for the Horizontal Register . . . 60
4.3.2 CTI Model for the Vertical Register . . . 61
4.4 CTI Measurements and Modeling . . . 67
4.4.1 Results on 2-phase CCDs . . . 67
4.4.2 Results on 3-phase CCDs . . . 70
4.4.3 Defect Identification and Annealing . . . 71

5 Methods for CTI Improvement 75
5.1 Timing of the Charge Transfer . . . 76
5.1.1 Readout Speed . . . 76
5.1.2 Clock Pattern . . . 78
5.2 Influence of the Signal Density . . . 82
5.2.1 Notch CCD . . . 82
5.2.2 Differences Between 2- and 3-phase CCDs . . . 84
5.2.3 Pixel Size . . . 86
5.3 Injection of Background Charge . . . 86
5.4 Pixel Occupancy . . . 90
5.5 Implications to the CCD Design . . . 92

Summary 95

Bibliography 97

Chapter 1

CCD Vertex Detector

1.1 Vertex Detectors in High Energy Physics

Determination of trajectories of charged particles, which are generated at secondary interaction points, spatially separated from the primary collision is of primary importance for the contemporary high energy physics experiments. The ongoing B-factory experiments in USA and Japan rely heavily on precision tracking to fulfill their scientific program. The experiments, planned at Fermilab, CERN and the future Linear Collider will require even more precise vertexing, performed by detectors of ever increasing precision, complexity and tracking power.

The purpose of the vertex detector is to measure the impact parameter of the tracks, defined as the distance of closest approach of the extrapolated particle trajectory to the interaction point and to separate the secondary and tertiary vertices from the primary vertex. The need for precise vertexing arises from the fact, that the object of modern high energy physics are mainly short-lived particles. For example, the lifetimes of the heavy b and c quarks and of the τ lepton are of the order of 1 ps, therefore spatial resolution of better than $\sim 100\mu$m is required. Such precision tracking can be provided only by solid-state medium, such as semiconductor detector. At least two measurements of the particle hits are required to find its trajectory by extrapolation and to determine the impact parameter. Modern vertex detectors contain more than 3 layers to ensure tracking with redundancy.

Microstrip and pixel detectors are widely used as tracking devices in fixed-target and collider experiments. Depending on the accelerator parameters, radiation backgrounds and the desired precision, one type of detector is preferred over the other. With the advances of semiconductor technology, pixel detectors are likely to be the choice for the

future experiments in spite of the increased complexity of the detectors. The detectors, which attract most of the attention are active pixel sensors (hybrid and monolithic) and Charge Coupled Devices (CCD).

The requirements and the parameters of a vertex detector follow from its function to measure precisely impact parameters and to resolve secondary and tertiary vertices from particles generated in the initial collision.

1) **Impact parameter resolution** σ_{IP}. It is specified with two terms, single point resolution (intrinsic spatial resolution) σ_{sp}, and multiple scattering term σ_{ms}, and is defined as:

$$\sigma_{IP} = \sigma_{sp} \oplus \frac{\sigma_{ms}}{p \sin^{3/2}\theta}, \tag{1.1}$$

where p is the particle momentum and θ is the polar angle. Usually the impact resolutions in the orthogonal $r\phi$ and rz projections are different and are specified separately as $\sigma_{r\phi}$ and σ_{rz}.

2) **Physical thickness**, measured in units of radiation length X_0. The detector should be thin to minimize multiple scattering. The RMS deflection in radians, caused by multiple scattering in a material of thickness t is given by [1]

$$\phi_{RMS} = \langle \phi^2 \rangle^{1/2} = \frac{zE_s}{pv} \left(\frac{t}{X_0} \right)^{1/2}, \tag{1.2}$$

where $E_s = \sqrt{4\pi \times 137}\, mc^2 = 21$ MeV, and

$$\frac{1}{X_0} = \frac{4Z(Z+1)r_e^2 N_A}{137A} \ln\left(\frac{183}{Z^{1/3}} \right). \tag{1.3}$$

Here p, v and z are the momentum, velocity and charge of the traversing particle, Z and A are the atomic number and mass number of the medium, N_A is the Avogadro's number and $r_e^2 = e^2/mc^2$ is the classical electron radius.

3) **Distance of the first detector layer to the interaction point**. The first layer provides the closest measurement of the tracks and helps reduce the multiple scattering term in the impact parameter resolution. The error from the extrapolation can be minimized by putting the first layer as close as possible to the interaction point.

4) **Polar angle coverage** – specifies the range of polar angles θ covered by the detector.

5) **Readout time**, which should be as short as possible.

1.2 CCD Principles and Operation

1.2.1 Introduction to CCDs

CCDs were developed in the 70s with the advances of MOS technology. Soon after that, they took over the vacuum tube as imaging devices, and now are widely used in video applications and digital photography. There are many excellent references, which describe the principles of CCD, for example the books by Beynon [2] and Theuwissen [3].

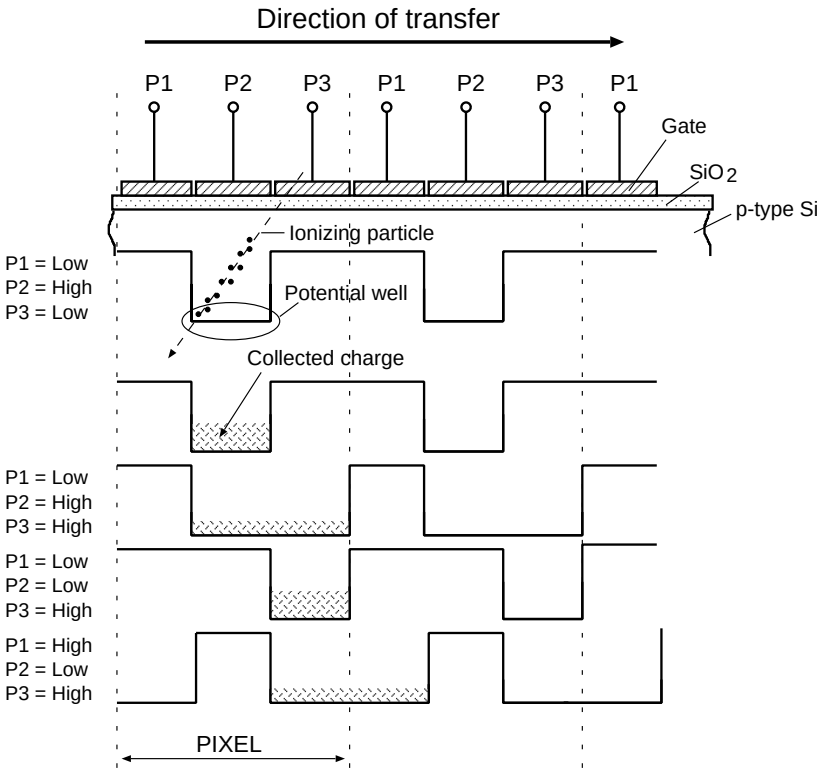

Figure 1.1: Generation, storage and transfer of charge in a 3-phase CCD.

In CCDs charge is generated and stored in potential wells, created under an array of closely spaced MOS capacitors. The concept of potential well derives from the operation of depleted MOS structure and it is very useful for understanding the principles of the CCD. In the MOS structure shown on Fig. 1.1, potential wells are created by applying bias to the gates and depleting the semiconductor underneath. Electrons, created by ionization from photons or traversing particles are collected and stored in the region under the gate, which is free of majority carriers. Holes, generated together with the electrons are dumped to the substrate and are not collected. Physically, electrons are stored very close to the Si-SiO_2 interface and not in the volume of the semiconductor. In the upper diagram on

Fig. 1.1 potential wells are created under the gates P2, whereas gates P1 and P3 serve as separators between the charges of neighboring pixels. Charge can be transported by changing the voltages at the gates so that the wells move from pixel to pixel. This is possible because of the charge coupling, provided by partially overlapping gates.

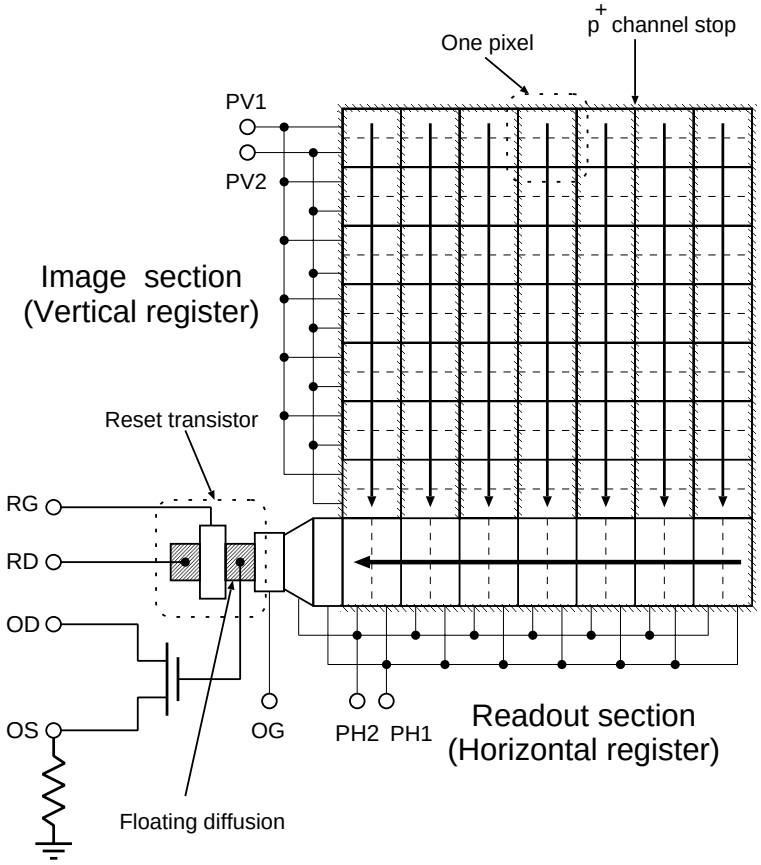

Figure 1.2: Diagram of a 2-phase CCD, containing 7×7 pixels.

A 2-dimensional CCD can be created by placing many structures together in a matrix (Fig. 1.2). To prevent charge from spreading between columns, additional p^+ implants (channel stops) are placed between them to electrostatically confine the electrons. Charge is transferred in parallel in the imaging section (vertical register) and serially in the horizontal register to the output. The 2- and 3-phase charge transfer structures are the most widely used architectures today.

Electrons are converted to voltage signal at the output node, which is typically a "floating" diffusion area on chip. The output node is connected periodically to V_{RD} by a reset transistor before the next charge reaches it. The voltage V_{RD} is sufficiently positive, so that the output node is attractive to electrons. The floating diffusion is buffered by

a MOS transistor in source follower configuration. The potential of the output node decreases when the electron packet reaches it, and that change represents the output signal, developed at the load resistor connected to OS. To achieve reasonable sensitivity, the node capacitance must be well below 1 pF, which requires that the reset and the output transistor should be placed on-chip. For a typical CCD sensitivity (conversion coefficient) of 1 μV/electron the capacitance of the output node is 0.16 pF. The output gate (OG) is held at fixed bias, which minimizes the electrostatic pick-up from the large clock pulses in the serial register.

In CCDs for video applications the charge is transported in separate shift registers between the photosensitive areas [3]. Only the full frame transfer CCD, shown on Fig. 1.2 is of interest as particle detector because 100% of its surface can be used as detector.

1.2.2 Buried Channel CCD

The CCD shown on Fig. 1.1 is named surface channel CCD (SCCD), because the electrons are physically stored and transported just under the the Si-SiO_2 interface. In the SCCD the charge is trapped by numerous interface defects and is transported with large losses.

This unwanted effect is eliminated in the buried channel CCD (BCCD) (Fig. 1.3). In the BCCD the potential minimum for electrons is situated several hundred nanometers away from the Si-SiO_2 interface by introducing additional n-type implant in the epitaxial layer. The charge does not interact with the interface and only trapping by bulk defects contributes to the transfer losses. The charge transfer losses of the BCCD are greatly reduced in comparison with the SCCD. Because of its ability to transport reliably very small signal packets, of the order of several electrons, the BCCD has become the dominant type of CCD for scientific applications. The charge transfer losses of modern BCCDs can be less than 10^{-5} per pixel.

1.2.3 Multi Pinned Phase CCD

For scientific applications it is often required to minimize the dark current of the CCD. The dominant source of dark current in BCCD are the defects at the Si-SiO_2 interface, however it can be suppressed by supplying free carriers to the interface by inversion or accumulation. In the BCCD on Fig. 1.3 the potential at the surface becomes negative and attractive to holes at $V_G < -4$ V as the interface is inverted, because holes are freely provided by the p^+ channel stops [4]. In this mode the surface potential is "pinned"

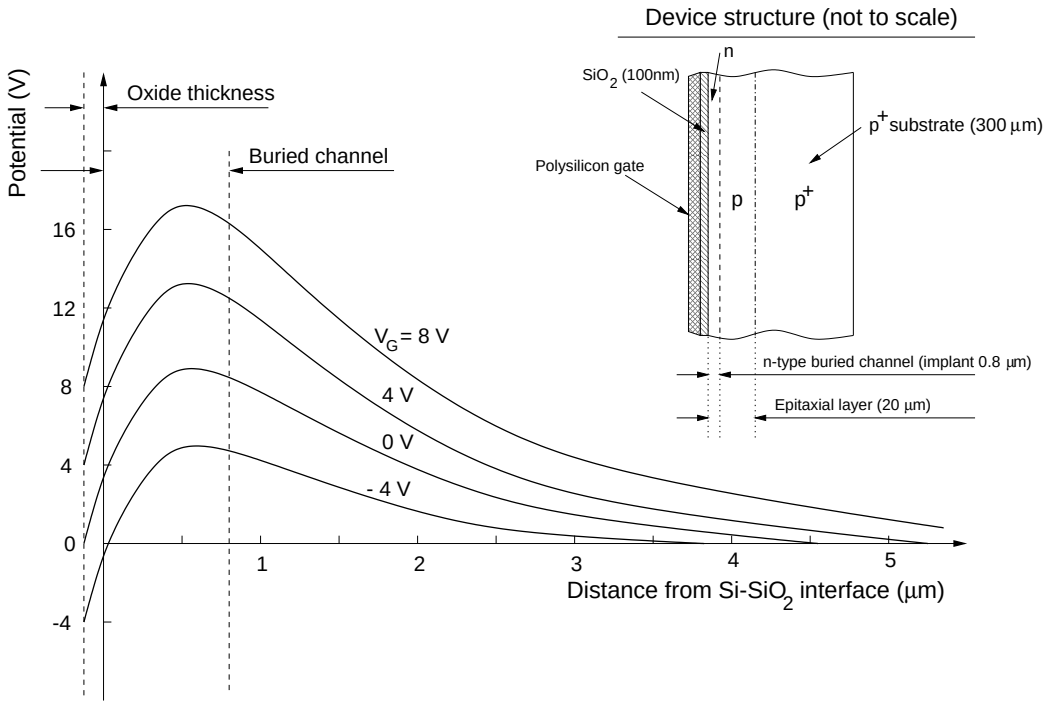

Figure 1.3: After [4], potential diagram of a buried channel CCD structure at different gate bias in a plane perpendicular to the surface. It should be noted, that only a fraction of the epitaxial layer is depleted. The inset shows the device structure in the same plane.

at substrate potential. Pinning is not possible during charge transfer, however if that period is much shorter than the integration time, the dark current will not deteriorate significantly. With the surface pinning technique it is possible to reduce the dark current of the CCD by at least one order of magnitude.

A potential barrier between the pixels is required to provide potential wells for charge collection during integration, when all the gates are equally biased. In Multi Pinned Phase (MPP) CCDs additional p-type implant is introduced under one of the gates of each pixel to provide the barrier. The 2-phase CCD has such a barrier built-in to give the direction of the transfer and is very well suited for MPP mode operation.

1.2.4 CCDs as Particle Detectors

CCDs offer several attractive properties for particle tracking applications. Before considering them, some important features of the CCD have to be mentioned. The first one is, that in contrast with the microstrip sensors, CCDs are non-equilibrium detectors [5]. The dark charge is collected in the potential wells together with the signal from traversing particles. This charge has to be removed periodically, which is done naturally in the

readout cycle. The parameters of the CCD sensors as particle detectors as a function of the dark current generation and readout speed are considered in [6].

Another feature of the CCD is that although only a part of the epitaxial layer is depleted (Fig. 1.3), the charge is generated and collected in its whole volume. This is possible because of the largely different doping concentration of the p^+-substrate and the p-epilayer, which creates potential barrier of about 100 mV at the interface. The electrons generated in the undepleted silicon diffuse to the substrate and are reflected by the barrier, which acts as a perfect mirror. They are consequently caught in the drift lateral field and collected in the buried channel. Charge is shared between neighboring pixels because some of the electrons difuse in the plane parallel to the CCD surface. This effect can be used for improving the point spatial resolution of the CCD to better than

$$\sigma_{residue} = \frac{pixel\ size}{\sqrt{12}} \tag{1.4}$$

by cluster centroid finding.

Because of the small thickness of the active volume, the CCD acts as dE/dx detector. The signal, generated by MIPs is about 60 e^-/μm at the peak of the Landau distribution and 108 e^-/μm on average. In 20 μm thick epitaxial layer this corresponds to relatively small signal of 1200 e^- at the peak. Due to the small capacitance of the output CCD node, signal to noise ratio is sufficiently high even with such a small signal.

The main advantages of the CCDs as particle tracking detector can be summarized as follows [7]:

1) True 2-dimensional point resolution;

2) Very good measurement precision ($\sim 4\mu$m) and 2-track separation ($\sim 40\mu$m);

3) High granularity (high number of pixels per unit area), which helps decrease the pixel occupancy and to tolerate high hit density and backgrounds;

4) Can be made physically thin to reduce the multiple scattering;

5) The number of pixels on a single device can be large ($> 10^6$);

6) Large area devices (> 10 cm^2) can be used.

In spite of the many attractive characteristics, the CCD has two disadvantages, inherent to its structure:

1) The readout is serial, therefore it is rather slow. This is not significant problem for linear e^+e^- colliders because of their low duty cycle, but it can be a great hurdle for applications in circular accelerators;

2) Vulnerable to radiation damage. The charge travels several centimeters from the point of its generation to the output and electrons can be trapped by numerous radiation-induced defects on the way.

1.3 CCD–based Vertex Detector

The VXD3 vertex detector at Stanford Linear Collider Fig. 1.4 is currently the most advanced CCD-based vertex detector. It is built with large area custom CCDs, each containing 4000×800 pixels with size of 20μm×20μm. Special measures has been taken to decrease the amount of material to 0.4% X_0 per ladder.

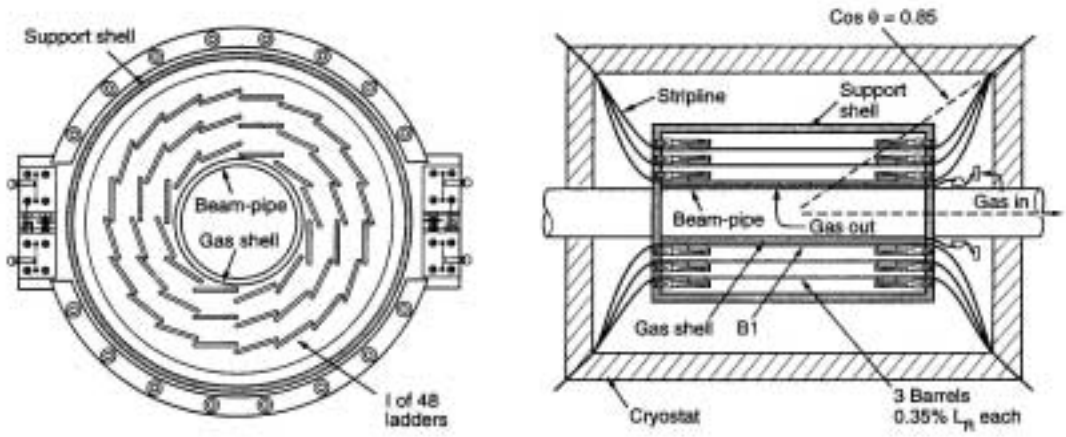

Figure 1.4: The VXD3 vertex detector at SLD ([7], p. 66). The device has 96 CCDs, each with an area of 8×1.6 cm^2, and a total of 307 million pixels.

The VXD3 has achived the world's best impact parameter resolution, measured in the orthogonal $r\phi$ and rz projections as [8]:

$$\sigma_{r\phi} = 14.0 \oplus \frac{33}{p \sin^{3/2}\theta} \ \mu\text{m} \tag{1.5}$$

$$\sigma_{rz} = 26.5 \oplus \frac{33}{p \sin^{3/2}\theta} \ \mu\text{m}. \tag{1.6}$$

For the future e^+e^- Linear Collider (LC) significant improvements should be made to reach the desired value [9]:

$$\sigma_{r\phi} \approx \sigma_{rz} \approx 4.5 \oplus \frac{5.5}{p \sin^{3/2}\theta} \ \mu\text{m} \tag{1.7}$$

Such high precision is required to meet the challenging physics program at the LC, which includes studies on the t-quark, mechanism of the electroweak symmetry breaking and searches for Supersymmetry. Measurements of the branching ratios of the decays of the Higgs boson to $b\overline{b}$, $c\overline{c}$ and $\tau^+\tau^-$ are important to determine its Standard Model or Supersymmetric nature [10]. These experiments heavily rely on precise measurements, provided by the vertex detector.

Because of the multijet final states, the mean track momentum is expected to be low ($\sim$ 1 GeV/c) even at very high energy of the colliding electron and positron beams [11]. At such low momentum the impact parameter resolution is dominated by multiple scattering, which requires further reducing the thickness of the detector to 0.12% X_0 per ladder [9].

Chapter 2

Radiation Damage Effects in CCDs

Soon after the beginning of the space age and nuclear arms race, scientists and engineers discovered that semiconductor devices are particularly sensitive to radiation, both ionizing and non-ionizing [12]. It was found, that the degradation of the parameters of bipolar and MOS devices is caused by radiation-induced surface effects at the Si-SiO_2 interface, as well as by defects in the bulk silicon.

Ionizing radiation creates electron-hole pairs in silicon dioxide, which is widely used as gate and field dielectric in contemporary MOS devices. These charge carriers drift in the electric field (externally applied of built-in) to the corresponding electrode. Electrons quickly reach the positive electrode, but some of the holes remain trapped in the oxide and generate radiation-induced trapped oxide charge, which can be stable for periods ranging from minutes to years.

At any Si-SiO_2 interface there are a number of interface traps, which result from the strained or dangling silicon bonds at the boundary between the two materials. Ionizing radiation causes the density of these traps to increase, giving rise to radiation-induced interface traps. The formation of radiation-induced trapped oxide charge and interface defects is referred under the term **surface damage**.

Radiation with sufficiently high energy can displace Si atoms from their lattice positions, creating displacement damage. This process affects the properties of the bulk semiconductor and it is known as **bulk damage**. Low energy electrons and X-rays can deliver only small energy to the recoil Si atom and mainly isolated displacements, or point defects, can be created. On the other hand, heavier particles, such as protons and neutrons can knock out Si atoms having sufficient energy to further displace atoms in the crystal. These secondary displacements form defect clusters, which have high local

defect density and can be tens of nanometers wide. Defect clusters often have complicated behavior and more damaging effect on the properties of semiconductor devices than point defects.

It should be noted, that CCDs are made of relatively high doped *device-grade* silicon. Radiation induced point defects and damage clusters in such material have been studied extensively in the past decades and significant knowledge about their properties has been accumulated. The more complicated radiation damage phenomena, arising from the presence of defect clusters in high-quality, low doped ($\sim 10^{12}$ cm^{-3}) *detector-grade* material are not relevant to CCDs and are not discussed in this thesis.

2.1 Surface Damage

2.1.1 Radiation-Induced Trapped Positive Charge

About 18 eV of deposited energy is required for the creation of one electron-hole pair by ionizing radiation in silicon dioxide. Some pairs recombine, but some of them drift in the oxide electric field. Those electrons, which escape recombination quickly reach the positive electrode because of their high mobility. Holes are much less mobile and with time undergo stochastic slow transport to the SiO_2 interface [12]. Electron mobility in SiO_2 at room temperature is ~ 20 cm^{2}V^{-1}s^{-1} and increases to ~ 40 cm^{2}V^{-1}s^{-1} at temperatures below 150 K. Therefore, for typical 100 nm thick oxide it takes ~ 5 ps for all electrons to reach the positive electrode, if the applied electric field is 10^5 V/cm. Hole mobility has been measured in the range 10^{-4} to 10^{-11} cm^{2}V^{-1}s^{-1}. Because it is many orders of magnitude lower than the electron mobility, hole transport through the oxide takes place in the time scale of seconds or hours. Over time, they move toward the negative electrode and some of them are captured by oxide traps within several nanometers from the SiO_2 interface. For positive bias (i.e., the gate is positive with respect to the silicon surface) holes are trapped near the Si-SiO_2 interface.

Trapped holes change the parameters of MOS structures in a way identical to applying an external voltage to the gate. The radiation-induced voltage shift ΔV_{ot} can be expressed as

$$\Delta V_{ot} = -\frac{q}{\epsilon_{ox}} d_{ox} \Delta Q_{ot}, \tag{2.1}$$

where ϵ_{ox} is the oxide permittivity, d_{ox} is the oxide thickness and ΔQ_{ot} is the change of the areal charge density at the Si-SiO_2 interface [12]. Because the flat band voltage

in MOS devices changes as ΔV_{ot}, the term flat band voltage shift is frequently used to describe this phenomenon. If holes are generated uniformly in the oxide by low intensity irradiation, then their fluence F_h toward the SiO_2 interface will be proportional to the oxide thickness d_{ox}:

$$F_h = K_g f_y D d_{ox}, \tag{2.2}$$

where K_g is the charge generation coefficient, f_y is the free charge yield and D is the radiation dose. If the fraction of radiation-induced holes that are trapped in the oxide is f_T, then ΔV_{ot} becomes

$$\Delta V_{ot} = -\frac{q}{\epsilon_{ox}} K_g f_y D f_T d_{ox}^2. \tag{2.3}$$

Equation 2.3 shows that one important way to reduce ΔV_{ot} is to decrease the thickness of the oxide. This method is widely used to manufacture "radiation hard" MOS devices. Another approach is to reduce the density of oxide traps, and therefore the ratio of trapped holes in the oxide by optimizing the fabrication process. In oxides, designated as "hard", the hole trapping factor f_T can be as low as 1%, while in "soft" oxides this ratio can be close to 100%.

Gate insulators, which use layers of SiO_2 and Si_3N_4 have successfully been used to reduce the radiation-induced flat band voltage shift. This dielectric system uses the ability of Si_3N_4 to capture electrons, which compensate to some extent for the effect of trapped holes [13].

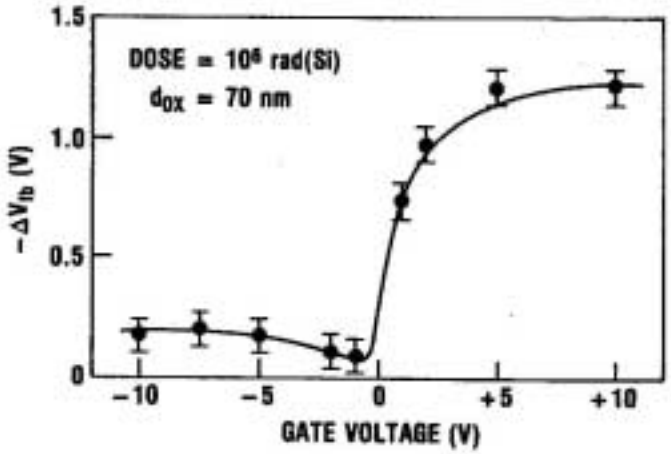

Figure 2.1: Bias dependence of the flat band voltage shift (from [12], p. 155).

During normal operating conditions, MOS devices are irradiated with some bias voltage applied to the gates. For positive bias, holes are transported to the Si-SiO_2 interface,

where they cause larger flat band voltage shift than if the bias was negative and they were trapped at the gate-SiO_2 interface. This important dependence has been observed experimentally by several authors ([12]-[14]) and an example experimental result is presented on Fig. 2.1. Furthermore, the ratio of holes, that do not recombine with electrons shortly after their generation increases with the applied electric field [12]. For zero field the recombination is at its maximum, therefore less holes are produced and less are later trapped in the oxide. Experimental results confirm, that zero bias during irradiation produces the smallest radiation-induced voltage shift [12][13].

Implications to CCDs

Gate bias in buried n-channel CCDs is negative, therefore the radiation-induced voltage shifts are not significant problem. Small flat band voltage shifts in the order of few volts can be accommodated by adjustment of the amplitude of the the gate drive voltages. However, a limitation can be imposed from the maximum allowed supply current and power dissipation in the gate drivers and the CCD chip, because the dissipated power is proportional to the voltage amplitude squared. As long as no parasitic effects from the increased pulse amplitude appear, the shifts are not a limitation for the device operation.

If the flat band voltage shifts are higher, the device can seize to function properly. Such a failure mode can be caused from parasitic charge injection from the input structures, or if the output node becomes negative to the potential of the output gate [15]. In the second case the electrons are not attracted to the output node. It is also possible that the output node cannot be reset to V_{rd} because of the threshold voltage shift in the reset MOSFET. Severe flat band voltage shifts can distort the shape of the potential wells and cause large charge transfer losses.

2.1.2 Radiation-Induced Interface Traps

Interface defects appear at the boundary between the crystalline silicon and the amorphous silicon dioxide during the growth of the SiO_2 by thermal oxidation. They result from strained or uncompleted silicon bonds at the interface. The density of the interface traps depends strongly on the processing parameters, such as oxidation temperature, and is usually in the range $10^9 - 10^{10}\mathrm{cm}^{-2}$.

Ionizing radiation can increase significantly their density and change their energy dis-

tribution. Interface traps are generated in at least two stages ([12], p. 241). A prompt component has been connected with direct interaction of radiation with the interface. There is at least one delayed component, which grows from seconds to days after irradiation. It depends on the oxide electric field, thickness, and processing. Interface traps anneal at temperature $> 100°C$.

Implications to CCDs

Interface traps are the dominant source of dark current in modern CCDs, because the generation rate at the Si-SiO_2 interface is higher than that in the epitaxial bulk silicon. Therefore, measures have to be taken to ensure as low as possible radiation-induced interface traps. These include mainly careful optimization of the manufacturing process. The surface dark current can be greatly suppressed by inverse biasing the Si-SiO_2 interface, which has been proposed by N. Saks as a method for radiation hardening of CCD imagers [16].

2.2 Bulk damage

2.2.1 Basic Mechanisms and Defects

The basic mechanisms of displacement damage and subsequent formation of electrically active defects have been summarized by Wunstorf [14] and Van Lint [17]. The irradiating particle collides with a Si atom, delivering sufficient energy to knock it out from its lattice site. The transferred energy is expressed as non-ionizing energy loss (NIEL) for the incident particle. If the displaced atom possesses high kinetic energy, it can knock out additional atoms. These further displacements take place in a small region, usually several tens of nanometers wide.

The so generated interstitial (knocked out) Si atoms and vacancies (empty lattice sites) can recombine and repair the initial defect; or the primary defects rearrange, migrate through the crystal, interact with impurities and form stable defect complexes. The electrically active stable defects on its turn influence the properties of bulk silicon by forming traps in the silicon band gap, which can capture and emit charge carriers.

If a defect results from the displacement of a single Si atom and subsequent rearrangement, it is called **point defect**. Closely situated multiple displacements, which can

interact electrically is called **defect cluster**. Light particles, such as electrons generate mostly point defects, and need more than 5 MeV to produce clusters [14]. The energy threshold for electrons to displace a Si atom has been estimated to $\sim$ 260 keV, whereas only 190 eV is requred for a neutron to do the same effect [5].

Heavy particles easily create clusters because of the high energy of the primary recoil Si atom. Neutrons, protons and pions need only about 15 keV to create clusters and generate point defects as well. The relative number of point defects is higher for protons and pions due to the repulsive Coulomb interaction [14]. A recoil Si atom needs about 5 keV of energy to displace other Si atoms in the crystal. Since these displacements are closely situated, most of them repair and only about 2% of all generated defects form electrically active states.

Vacancies migrate in the crystal and form stable, electrically active defect complexes by interaction with the impurities such as oxygen, phosphorus and carbon, or with themselves. The schematic description of the stable defect complexes is presented on Fig. 2.2.

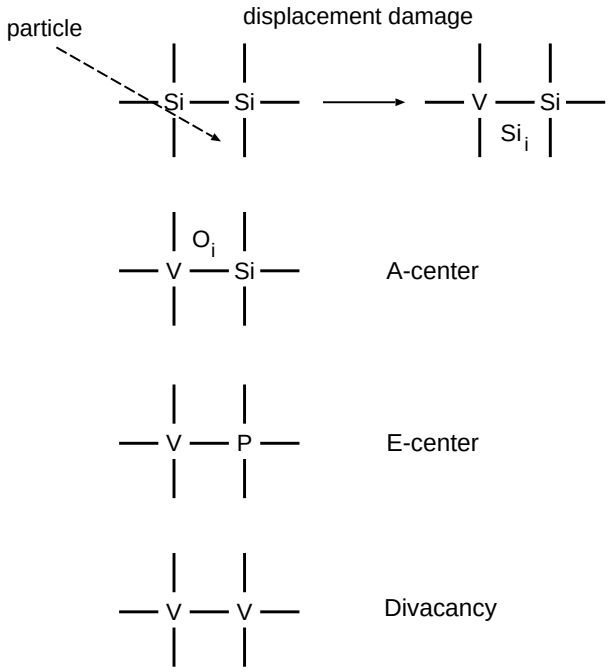

Figure 2.2: Irradiation-induced defect complexes in n-type silicon.

The reactions between vacancies (V), interstitial (i) and substitutional atoms (s), leading to creation of defects complexes, can be expressed as follows:

$particle + Si_s \rightarrow Si_i + V$ (displacement damage)

$O_i + V \rightarrow O - V$ (Interstitial O + Vacancy $\rightarrow$ $A-$center)

$P_s + V \rightarrow P - V$ (Substitutional P + Vacancy $\rightarrow$ $E-$center)

$V + V \rightarrow V - V$ (Formation of Divacancy)

$Si_i + V \rightarrow Si_s$ (Interstitial Si + Vacancy $\rightarrow$ Substitutional Si, or defect repair)

Type and energy of radiation are very important when considering the radiation damage effects in CCDs, because of the above mentioned differences between the spatial defect distribution.

In CCDs, charge is stored and transported in the buried channel, which is n-type, phosphorus doped epitaxial silicon. The usual dopant concentration at the surface of the wafer is about 10^{16} cm^{-3}, however the doping at the potential minimum of the channel is at least one order of magnitude lower because of the doping profile. The most important radiation-induced defects, observed in such material are the $A-$center, the divacancy $(V - V)$ and the $E-$center. The $A-$center has been identified as a vacancy-oxygen complex at $\mathrm{E_c} - 0.18$ eV and $\sigma_n = 10^{-14}$ cm^2. The divacancy has two states, one of them at $\mathrm{E_c} - 0.41$ eV with $\sigma_n = 2 \times 10^{-15}$ cm^2 (single charged when occupied, $V - V^{0/-}$). The other one, doubly charged when occupied $(V - V^{-/=})$ has significantly smaller capture cross section of $\sigma_n = 4 \times 10^{-16}\exp(-0.017/kT)$ cm^2 and is situated at $\mathrm{E_c} - 0.25$ eV. The $E-$center is a phosphorus-vacancy complex, situated at $\mathrm{E_c} - 0.456$ eV, with $\sigma_n = 4 \times 10^{-15}$ cm^2. The most important results and data from studies on radiation-induced bulk defects in n-type silicon during the last 25 years, along with some experimental conditions are presented in Table 2.1.

The dopant and impurity concentrations play important role for the creation of different radiation-induced defect complexes. Several work have shown the importance of oxygen concentration on the formation of radiation-induced effects, for example [21]. Concerning the creation of the $E-$center, the reaction $P_s + V \rightarrow P - V$ is suppressed by the competitive $O_i + V \rightarrow O - V$ reaction in samples with high oxygen content. This result is confirmed by the observation, that the E center is dominant in FZ silicon

(low oxygen content $\sim 10^{15}\mathrm{cm}^{-3}$), but much smaller in CZ silicon (high oxygen content $\sim 10^{17}\mathrm{cm}^{-3}$). Modern CCDs are built on epitaxial Si, which has very low oxygen concentration ($< 10^{15}\mathrm{cm}^{-3}$) when grown, however during the production some oxygen diffuses from the oxygen-rich CZ substrate.

In the work of Tokuda *et al.* [20] it has been shown, that more $E-$centers are produced in silicon with higher phosphorus doping. In neutron-irradiated FZ silicon, doped with 4.5×10^{15} cm^{-3}, the E-center accounts for about 50% of the total concentration of the observed defect at $\mathrm{E_c} - 0.39$ eV, while in the 1.2×10^{16} cm^{-3} doped sample it is about 60%. The remaining part has been attributed to the divacancy.

The most widely used technique for study of radiation-induced bulk defects is the Deep Level Transient Spectroscopy (DLTS) [28]. DLTS is used to measure the energy positions, capture cross sections and concentration of defects. Determination of defect concentrations in high resistivity Si by DLTS has to be done with caution, because the dopant and defect concentrations can be comparable, which can distort the results [29].

Because the $E-$center and the divacancy are energetically situated very close in the band gap, they usually create a common peak in the DLTS spectra. Experimental separation of the contributions of each defect only be DLTS can be difficult, therefore annealing studies are often performed to clarify that issue. It is well known [19]-[21], that the $A-$center anneals at $\approx 350°$C, the divacancy at 300°C and the $E-$center at 150°C. By carrying out isochronal anneals with increasing temperature, it is possible to determine the contribution of the $E-$center and the divacancy to the common DLTS peak they form.

From the published results on irradiation damage effects in n-type silicon and CCDs, the following conclusions can be made:

1) The dominant radiation-induced defects in low resistivity, low oxygen content silicon (e.g. in the CCD buried channel) are the $A-$center and the $E-$center;

2) The concentration of the divacancy is generally smaller, however it may be important in oxygen-rich silicon, in which the formation of $E-$centers has been suppressed;

3) In low resistivity silicon (high phosphorus doping), irradiation by electrons and neutrons produces very similar or indistinguishable macroscopic effects.

2.2.2 Dark Current and Charge Transfer Losses

Bulk defects cause increased dark current in CCDs, and when irradiated by heavy particles, dark current non-uniformity (spikes) can also appear. Another very important damage effect is the loss of signal charge during transfer, or Charge-Transfer Inefficiency (CTI), caused by trapping of charge carriers by bulk defects.

Dark Current

Increase of the mean bulk dark current in CCDs has been observed by many authors [24], [30]-[33]. Mostly defects, situated near the midgap level ($\approx E_c - 0.55$ eV) contribute to this effect because of the exponential dependence of the dark current on the defect level. Dark current is an issue only for near-room temperature operation or long integration times, because it can be reduced to negligible values by cooling. As was mentioned before, the dominant source of dark current in buried-channel CCDs is the generation at the Si-SiO_2 interface. For devices operated with inverted surface potential, the interface component of the dark current is suppressed and only the bulk dark current is important.

Irradiation with heavy particles (e.g. protons, neutrons) often creates large non-uniformities in the dark current spatial distribution in the CCDs [24][33]. These non-uniformities, also known as "dark current spikes" or "hot pixels" manifest themselves as pixels with much higher dark current than the average CCD dark current. Their presence has been connected with the high electric fields caused by the device architecture and field-enhanced emission, the cluster nature of the radiation damage and crystal strains. Dark current spikes have great consequences in high temperature applications. Additionally, some of them show random fluctuations of the generated current, or Random Telegraph Signals (RTS) [34] [35].

Charge Transfer Losses

One of the most important issues is the charge losses, caused by trapping by bulk defects. The basic mechanism has been explained [36] by the different time constants and temperature dependence of the electron capture and emission processes. The capture time constant is usually of the order of several hundred nanosecods, depends as $1/x$ on

the charge density and has weak temperature dependence. The emission time constant varies from seconds to microseconds as the temperature increases, depends on the energy position of the defect but not on the signal density.

The CTI is a measure of the transfer efficiency, hence the losses caused by trapping. At low temperature, the emission time constant of the defects can be very large, of the order of seconds. Once a defect has captured an electron (which can be generated by ionization or thermally), the trap remains occupied for a time, much longer than the charge shift time, which is usually in the order of microseconds. Therefore, the defects cannot capture signal electrons and the CTI at low temperature is small. At high temperature, the emission time constant becomes small and comparable with the charge shift time. Trapped electrons are able to join their signal packet, because most of them are emitted already during the charge shift time, and the CTI is small again. At temperatures between these two extremes there is a peak in the CTI value.

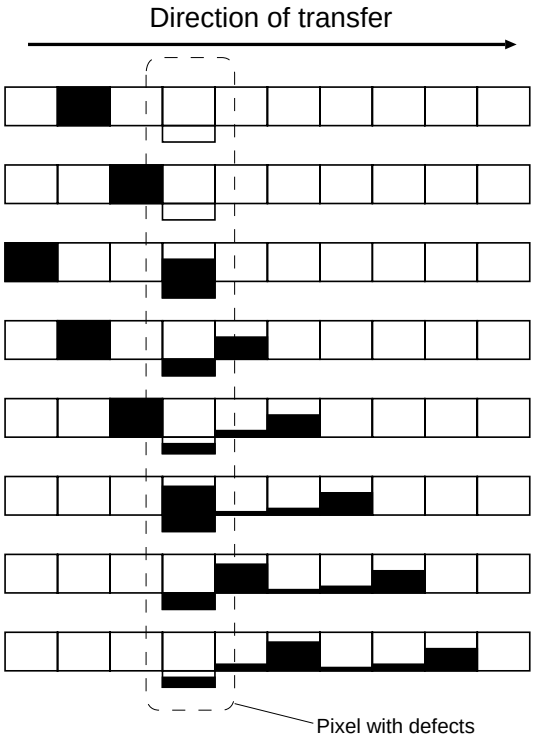

Figure 2.3: Schematic representation of mechanism of the charge transfer losses. For simplicity it has been assumed, that only one pixel contains defects. The second signal packet loses less charge, because the traps have been partially filled by the first signal packet.

The mechanism of charge transfer losses is illustrated on Fig. 2.3. When the signal

packet encounters traps, some of its electrons are captured and later released. Those electrons, which are released in trailing pixels do not join their original signal packet and account for the CTI. If a charge packet enters a pixel, in which part of the traps has been occupied, less electrons can be trapped and therefore less charge can be lost. Figure 2.3 shows, that there is no universal measurement of the CTI, because of the dependence on the pixel occupation, i.e. on the spatial density of the signal packets and on the trap filling. Therefore, pixel occupancy is an important parameter for every CTI measurement.

It is possible to correct partially for the CTI by summing the charge of several consecutive pixels. In reality, traps are uniformly distributed across the CCD, which makes the charge trail to extend for tens or hundreds of pixels, and such a correction is practically inapplicable because the noise is also added.

One is often interested not only in the CTI value, but in the total losses the charge suffers after all the transfers it takes to reach the output. The initial generated charge (or number of electrons) Q_0 is attenuated to Q_1 after one transfer:

$$Q_1 = Q_0(1 - CTI). \tag{2.4}$$

If the charge is transferred n times, the output charge Q_n is given by

$$Q_n = Q_0(1 - CTI)^n. \tag{2.5}$$

As will be shown later, CTI is a function of the size of the transported charge and (2.5) is valid only if CTI $\ll 1$. This dependence shows, that both the CTI and the number of transfers have to be considered for minimizing the charge transfer losses.

Table 2.1: Parameters of the most important radiation-induced defects in n-type, phosphorus-doped silicon. The dopant concentration is n_d. Most studies have identified defects by annealing. (Note: FZ = Float Zone Si, CZ = Czochralski grown Si, NTD = Neutron Transmutation Doped Si, CCD = measurements on CCD)

$A-$center	Divacancy	$E-$center	Conditions	Ref.
observed	–	$E_c - 0.44$ eV	FZ Si, annealing $n_d = 5 \times 10^{15}$ cm^{-3} 1 MeV electrons	[18]
$E_c - 0.18$ eV	$E_c - 0.39$ eV	$E_c - 0.44$ eV	CZ Si $n_d = 6 \times 10^{15}$ cm^{-3} 10 MeV electrons	[19]
$E_c - 0.15$ eV	$E_c - 0.39$ eV	$E_c - 0.39$ eV	CZ Si $n_d = 1.2 \times 10^{16}$cm^{-3} 2 MeV electrons, neutrons	[20]
$E_c - 0.17$ eV	$E_c - 0.413$ eV	$E_c - 0.456$ eV	NTD FZ Si ~ 60 Ω.cm 1 MeV, 12 MeV electrons	[21]
$E_c - 0.17$ eV	$E_c - 0.43$ eV	not observed	FZ Si, oxygen rich ~ 70 Ω.cm 1.3 MeV electrons	[22]
$E_c - 0.14$ eV	$E_c - 0.41$ eV	$E_c - 0.41$ eV	CZ Si, CCD $n_d = 2 \times 10^{16}$cm^{-3} $\sim$15 MeV neutrons	[23]
–	–	$E_c - 0.42$ eV	CCD annealed at 150°C 1.25 MeV ^{60}Co γ-rays	[24]
?	–	$E_c - 0.47$ eV	CCD annealed at 150°C ^{90}Sr β source	[25]
$E_c - 0.12$ eV(?)	–	$E_c - 0.42$ eV	CCD 10 MeV protons	[26]
$E_c - 0.17$ eV dominant	$E_c - 0.42$ eV	$E_c - 0.42$ eV	CCD $n_d = 10^{14}$ cm^{-3} 10 MeV protons	[27]

Chapter 3

Experimental Results on Irradiated CCDs

3.1 Experimental Setup and Measurement Techniques

3.1.1 Investigated CCDs

The experiments were carried out on two types of devices: the S5466-type two-phase CCDs, manufactured by Hamamatsu Photonics, Japan [37], and the three-phase CCD02-06, produced by Marconi Applied Technologies (former EEV Ltd), U.K. [38]. Both Hamamatsu and EEV CCDs are buried channel, Full-Frame Transfer (FFT) devices and have MPP mode capability. The CCD02-06 uses Advanced Inverted Mode Operation (AIMO) to achieve low dark current with smaller reduction of the full well capacity. The main parameters of the CCDs are given in Table 3.1.

Table 3.1: Parameters of the CCD Sensors.

Parameter	S5466	High Speed S5466	CCD02-06
Clock type	2-phase	2-phase	3-phase
Epitaxial layer	10μm	10μm	20μm
Pixel size	24μm×24μm	24μm×24μm	22μm×22μm
Active pixels	512(H)×512(V)	256(H)×256(V)	385(H)×578(V)
Total pixels	532(H)×520(V)	276(H)×264(V)	407(H)×578(V)
Sensitivity, μV/e$^-$	2.0 (typ.)	1.0 (typ.)	1.0 (typ.)
Dark current, e$^-$/s/pix	2.0 @ −20 °C	2.0 @ −20 °C	1.0 @ −20 °C
Readout noise, e$^-$ RMS	15 @ 78 kpix/s	50 @ 78 kpix/s	8 @ 20 kpix/s
Output	1-stage	2-stage	1-stage
Readout frequency	max. 1 MHz	max. 10 MHz	max. 3 MHz

Most of the measurements were performed on the S5466 CCD. Additionally three devices, based on the S5466 design were ordered from Hamamatsu Photonics and tested.

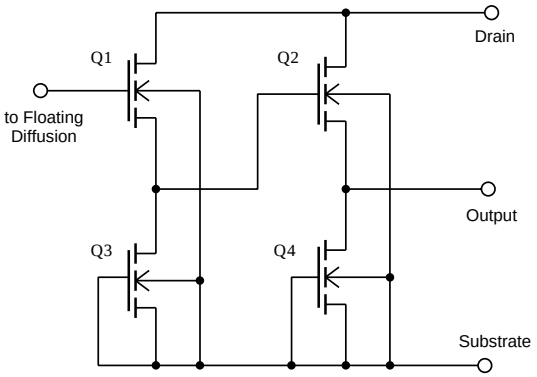

Figure 3.1: The output circuit of HS S5466 CCD.

The first one, High Speed S5466 CCD (HS S5466) can be operated at readout speed to 10 Mpix/s due to the two-stage source follower used for the output circuit (Fig. 3.1). The HS S5466 does not require external load resistor because of the constant current source, built with the transistor Q4.

Another Hamamatsu CCD (ONO CCD) uses the $SiO_2 - Si_3N_4 - SiO_2$ system as gate dielectric for reduction of the radiation induced flat-band voltage shifts. The thicknesses of the SiO_2 and Si_3N_4 layers are 55 nm and 70 nm, correspondingly. This CCD has 15μm thick epitaxial layer, 256(H)×256(V) pixels, higher dark current (20 e^-/s/pix @ −20 °C) and sensitivity of 1.5 $\mu V/e^-$. The other parameters are identical to the S5466 CCD.

The third custom CCD (Notch CCD) has an additional 3 μm−wide implant (or "notch") in the channel. This CCD features reduced CTI due to the smaller charge transport volume, as will be explained later in Section 5.2.1. The other parameters are the same as of the S5466 CCD.

3.1.2 Experimental Setup

The experimental setup is shown on Fig. 3.2. The CCD is mounted in a vacuum cryostat, model DET-1651-CCD, custom made by CRYO Industries of America, Inc. Changes were made to the original design to accommodate two 19-pin connectors in close proximity to the CCD. Temperature controller is NEOCERA LTC-11, which uses a silicon diode sensor for temperature regulation and an additional Pt resistor for monitoring, mounted in the

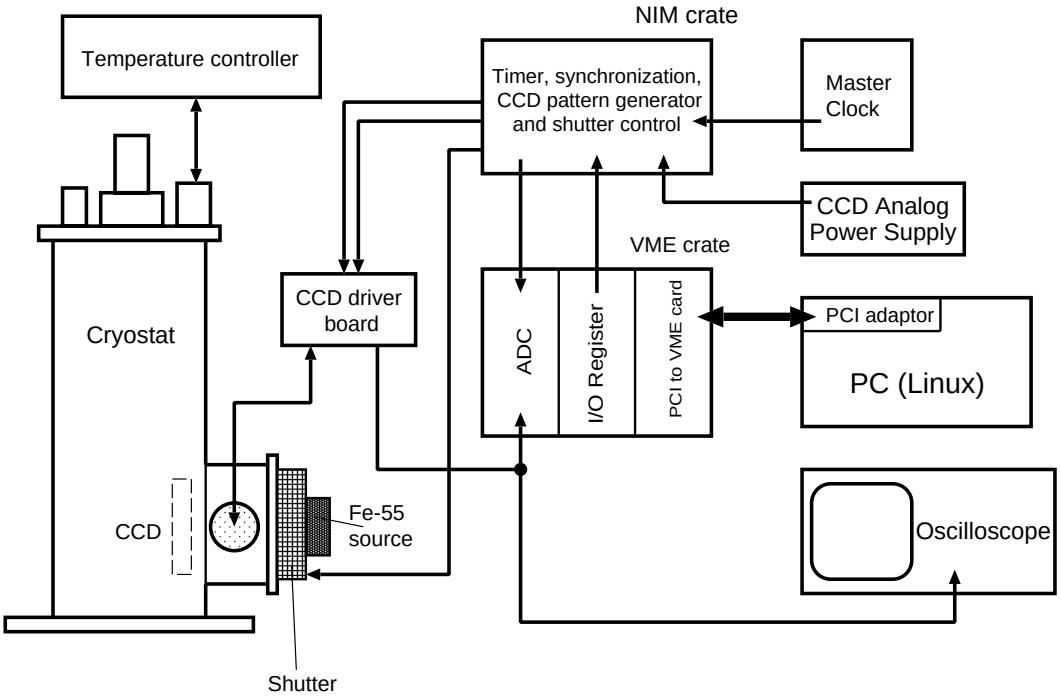

Figure 3.2: Experimental setup for CCD measurements.

sample holder near to the CCD.

The CCD driver board produces all the necessary DC biases and pulses for CCD operation. The clock pulses sequence is generated by the pattern generator, which has TTL compatible outputs. These signals are converted into bipolar pulses in the CCD driver board. The amplitude of the CCD drive pulses and DC bias voltages can be adjusted either by on-board variable resistors or externally supplied voltages. The CCD driver board amplifies the CCD output signal approximately 50 times using Correlated Double Sampling (CDS) amplifier. The output of the amplifier is fed to a 20 MSPS 12-bit ADC (Pentland MPX201A) and to oscilloscope, used for signal monitoring. The CCD clock sequence and the ADC acquisition are synchronized to the Master Clock generator (NF Electronic Instruments model 1610).

The experiment is controlled by a Linux-running PC (Pentium *III* 450 MHz, 128 MB) via VME interface. The PCI to VME bridge cards are BIT3 model 616. The computer maps and addresses the VME I/O register and the ADC memory and registers as part of its main memory [39]. The VME I/O register is used for generation of appropriate signals to control the acquisition process, loading of the NIM timer with the value for *CCD Start* period and for shutter control. The PCI-VME interface can provide continuous data

transfer of 2 Mbytes/s. In earlier experimental setup, a 66 MHz VME computer (model HP 743, running HP-RT) was used for control of the VME crate and ADC readout. The data was transferred by Ethernet to another HP-UX machine and analyzed. This setup was used at KEK and Saga for most of the measurements and later replaced by the more advanced PCI-VME interface. The basic block setup for both configurations is the same. Since the PC-based system is superior to the HP-based configuration, only the former is described here.

In both configurations the UNIDAQ V2.3 data acquisition system [40] was used. UNIDAQ allows on-line visualization and processing of the experimental data. This feature was used during measurement to control and adjust the experimental conditions, as well as to get preliminary results. The main data processing was done off-line, using data recorded on the hard disk of the PC, or to a tape robot at the Computer Center of KEK. In case of PC the data backup was done on DDS3 tapes.

The block connections of the NIM and VME modules are shown on Fig. 3.3. The Timer module has two functions: (a) to divide the master clock frequency and to supply clocks to the Pattern Generator and the ADC; and (b) to generate *CCD start* pulses with programmable period. The first function is accomplished simply by a 4-bit counter (74AC161) and a rotary switch. The timer function is implemented by a 12-bit counter (with 100 Hz clock input) and a 12-bit shift register, which holds the maximum count value of the counter. The shift register is loaded serially from outputs 5 and 6 of the VME I/O register. A short *CCD Start* pulse appears every time the counter reaches the value stored in the shift register. The period of the generated *CCD Start* signal can be programmed from 0.01 s to 99.9 s.

In the Pattern Generator the clock frequency is divided by 2, 4, 6 or 8 to form the subdivisions of the horizontal clock timing. The pulse pattern for the CCD drive circuit is synchronized to the Master Clock and the ADC Clock, and it is generated every time *CCD Start* arrives. The desired output pattern can be selected by a DIP switch from 8 sequences, programmed in two EPROMs. The output D14 generates synchronizing signal at the beginning of each horizontal sequence. It can be delayed by the Gated Generator 2 (GG2). If the computer has allowed next cycle by releasing *Veto* of GG3, GG3 triggers and forces *ADC Sync* LOW to allow ADC acquisition. GG4 is retriggered at the beginning of each horizontal row sequence, generates HIGH *Veto* signal to GG3 and does not allow

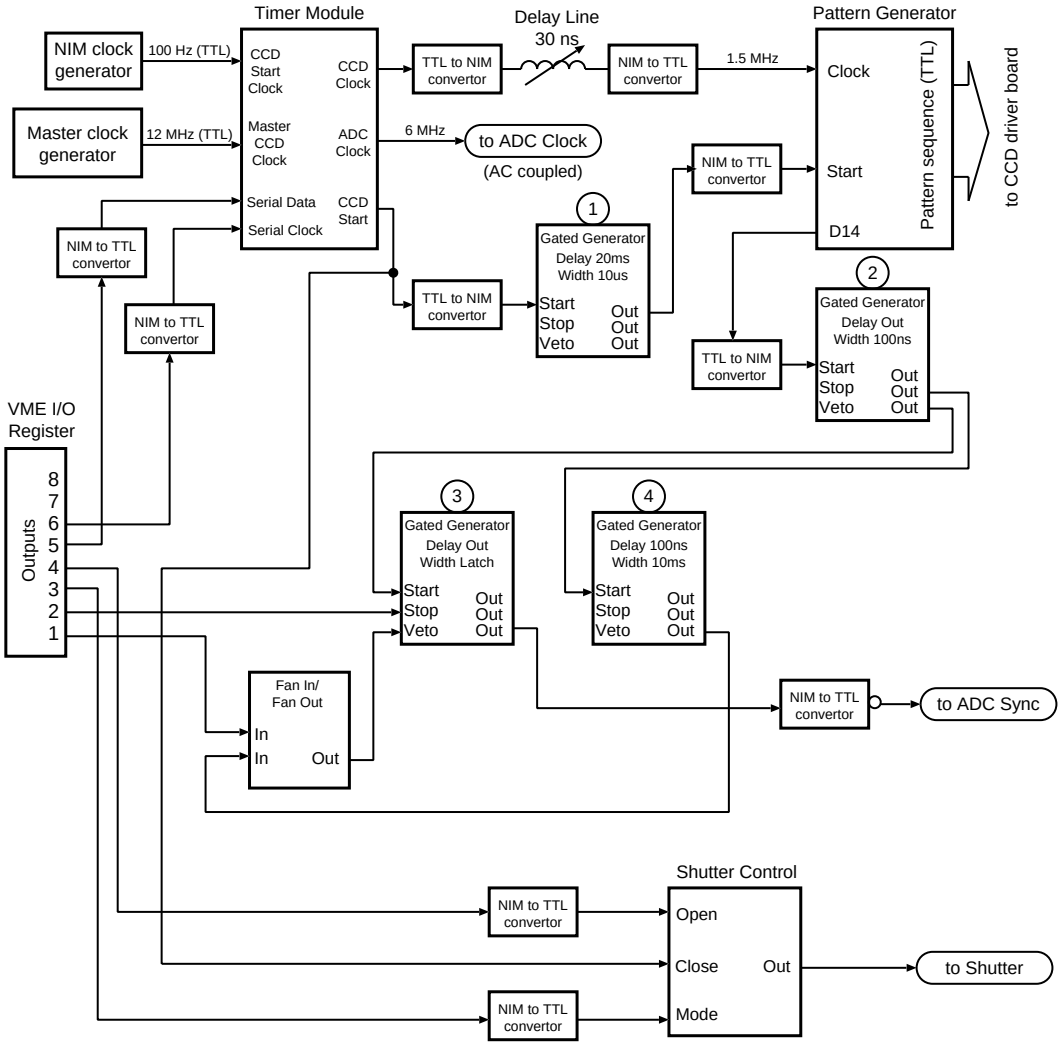

Figure 3.3: Block connections of the experimental setup. The settings are shown for readout speed of 250 kpix/s, with the internal divider of the Pattern Generator set to ÷6.

unwanted transitions of the *ADC Sync* during readout.

Every *CCD Start* pulse closes the shutter to prevent X-rays from reaching the CCD during readout. The shutter is opened after the readout cycle by a pulse from the VME I/O register. If *Mode* is HIGH, the *Close* signal is disabled and the shutter remains open. GG1 delays the *Start* signal to the Pattern Generator by ≈20 ms, which is slightly longer than the shutter close time. This is done to ensure that the shutter is closed at the beginning of the CCD readout.

After the CCD frame is transferred from the ADC to the computer memory, the raw ADC information was processed on-line in the following way:

1) The two consecutive 12-bit ADC samples are separated from their 32-bit word;
2) The samples are converted from two's complement format to unsigned integer;
3) The data is converted from 1-dimensional serial format to 2-dimensional format, corresponding to the 2-D pixel array of the CCD;
4) The average value of the horizontal overclock pixels (*hovcl*), used as a reference, is subtracted from every pixel from the same horizontal row.

The result of this processing is a 2-dimensional array, containing the charge in ADC units (ADU) of the active pixels of the CCD. The data contained in this array is used for all the following measurements.

3.1.3 CTI Measurement

The CTI of the vertical and the horizontal registers of the CCD was found in 2 steps. First, several CCD frames without any illumination ("dark frames") were recorded and the average dark signal of each active pixel was stored to file. The standard deviation of the dark current σ_{dark} was determined from these dark frames with fitting by PAW [41] with a Gaussian. The value of σ_{dark}, obtained from the fit was used for the selection of isolated pixel events (IPE).

The second step is to subtract the recorded dark charge frame of each pixel from the CCD frames, obtained under X-ray illumination. This is especially important at high temperatures or in case of heavily irradiated CCDs because of the large dark current non-uniformity between the pixels. The IPE are separated from the subtracted frames, which contain X-ray generated charge plus dark current noise. A charge is considered to be an isolated pixel event, if it satisfies the following conditions:

1) The charge is above the selectable threshold,
2) The charge of the surrounding 8 pixels is not greater than $3\times\sigma_{dark}$.

This ensures that the IPE are spatially separated by at least one pixel, and significantly reduces the contribution of split events. The density of the IPE was kept small to get results close to the experimental conditions at the vertex detector. As will be shown later, the density of IPE can change dramatically the measured CTI values at low temperature.

The CTI is determined by observing the charge losses of IPE as the signal packet is

transported in the CCD registers. Only IPE, containing charge within the window of the 5.9 keV Mn-K_α line are taken into account. The charge is plotted versus the number of the pixel where it originates separately for the vertical and the horizontal register. The CTI is obtained from the slope of the scatter plot, which has been averaged over many frames (100 or more) to improve the statistics. The accuracy of this method is estimated to be better than 10^{-5} for nonirradiated devices.

It should be noted, that it is not necessary to calibrate the CCD (i.e., to know the correspondence between charge and ADU) for the CTI measurement.

3.1.4 Dark Current Measurement

The dark current was measured by taking several dark frames at different integration times. The dark charge of the active pixels was averaged over several frames for each integration time and the average pixel charge was plotted versus time. The dark current is obtained from the slope of the curve.

The gain of the system (expressed in electrons per ADU) was calibrated using the ^{55}Fe source. The temperature range for the CTI and dark current measurements was from $-100°$C to $+20°$C. A miniature platinum resistor was attached to each CCD or to the cold finger near to the CCD for better temperature monitoring.

3.1.5 CCD Irradiation

The CCDs were irradiated by electrons from a 9.7-mCi ^{90}Sr source at room temperature. All the CCDs were irradiated unbiased with their pins grounded through conductive rubber, except one device, which was biased and clocked.

The irradiation rate was calculated as $(1.4 \pm 0.2) \times 10^{10}$ cm^{-2}h^{-1} from geometrical considerations. A calculation of the dose rate in the S5466 CCD was done by measuring the average current in the reset drain node I_{rd} during electron irradiation. This current is a measure of the energy deposition of the irradiating β-electrons [15]. The energy deposition per unit mass and unit time in the epitaxial layer is given as the number of the generated electron-hole pairs, multiplied by the energy, needed to create them (taken as 3.6 eV):

$$E_{epi} = \frac{I_{rd}}{q m_{epi}} \times 3.6\ eV, \tag{3.1}$$

where q is the electron charge and m_{epi} is the mass of the epitaxial layer. The mass of the

CCD epitaxial layer m_{epi} with thickness $d = 10$ μm and area $S = 1.59$ cm^2 is given by

$$m_{epi} = \rho d S = 3.7 \times 10^{-3}\ g, \tag{3.2}$$

where $\rho = 2.33$ g/cm^3 is the density of silicon. With the leakage current subtracted, the reset drain current I_{rd} under continuous readout condition was measured to be 3.1 ± 0.2 nA. Since one rad is defined as $6.27{\times}10^7$ MeV/g, the irradiation rate R was calculated as

$$R = \frac{6.27 \times 10^7\ MeV/g}{E_{epi}} = 1080 \pm 65 \text{ rad/h}. \tag{3.3}$$

The same geometry was kept throughout all the irradiation steps to ensure the repeatability of the dose rate. This measurement was carried out on an undamaged device for a short time to ensure that the radiation damage effects do not cause any error to the experimentally determined values.

An ^{252}Cf source with an emission of $4.6\ {\times}10^5$ s^{-1} was used for the neutron irradiation. The average neutron energy for this source is 2 MeV. Under the same geometrical conditions as of the electron irradiation, the neutron fluence was estimated to be $(1.5{\pm}0.2){\times}10^7$ cm^{-2} h^{-1}.

3.2 Ionization Damage Effects and Dark Current

All the radiation damage effects, described in the previous chapter were observed in the irradiated CCDs. The experimental results in this section are presented in 4 subsections, according to the radiation damage effects in CCDs: flat band voltage shifts, interface and bulk dark current, spurious dark current and hot pixels.

3.2.1 Flat Band Voltage Shifts

A convenient method of measuring the flat-band voltage shift in MPP mode CCDs is to observe the change of the voltage, needed to invert the Si-SiO_2 interface. This voltage is negative referred to the substrate, therefore after buildup of positive charge in the oxide, the applied gate voltage increase in absolute value. For n-channel CCDs, the electric field in the oxide is pointed towards the gates so that holes are trapped mostly at the gate-SiO_2 interface, where they have less impact on the MPP threshold voltage than if they were trapped at the Si-SiO_2 interface.

The MPP threshold voltage can be found by measuring the dark current of the CCD at fixed temperature as a function of the gate bias voltage of the vertical register V_{ee}^{V} during the integration period. The threshold is determined as the voltage, at which the dark current abruptly decreases, indicating that inversion has been reached. The dark current of the CCD is generated almost entirely in its imaging section because of the long integration time. The dark current, generated in the horizontal register is about 2 orders of magnitude smaller because of the shorter readout time. For example, for a CCD pixel format with 576(H)×552(V) pixels (including the nonactive pixels and the overclocks) and readout speed of 250 kpix/s, the total readout time is 1.272 s and the horizontal shift time is 2.3 ms. The CCD integration time was usually set to 2.0 or 3.0 seconds. For this reason, the operating voltage of the horizontal register V_{ee}^{H} was kept unchanged. To avoid unwanted charge generation and injection from the input structures of the registers, the input gates of the S5466 devices were biased to V_{ee}^{V} and V_{ee}^{H}, correspondingly.

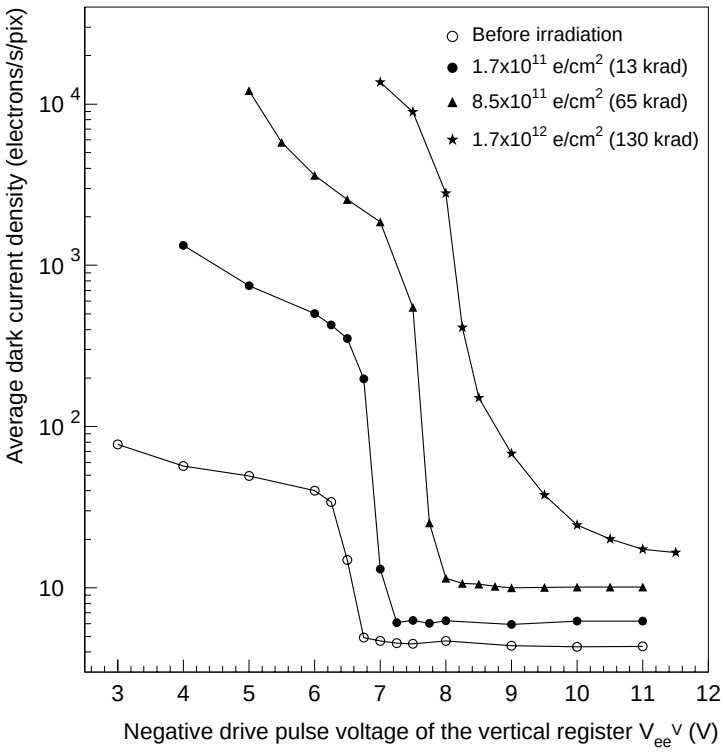

Figure 3.4: Average dark current density as a function of the electron irradiation and of the negative drive pulse voltage V_{ee}^{V} at −26°C, V_{ee}^{H} = -8.0 V. The device is S5466 #JS14/026, irradiated unbiased.

The shift of the threshold voltage V_{ee}^{MPP} for a S5466 device irradiated with its pins grounded is shown on Fig. 3.4. It can be noticed, that after irradiation to 1.7×10^{12} e^-/cm^2 the transition into MPP mode is not abrupt. This behavior can be explained by non-uniformity of the irradiation and the flat-band voltage shifts, which lead to spread in the threshold V_{ee}^{MPP} in pixels at different distance from the center of the CCD. The radial distribution of the V_{ee}^{MPP} was confirmed by measuring the dark current from different parts of the image.

One of the devices was irradiated to 4.3×10^{12} e^-/cm^2 and its V_{ee}^{MPP} threshold was well above 11V, which exceeded the safe limit of the MOS drivers. The swing of the clock pulses in the experiments is limited by the maximum supply voltage of the MOS drivers (MAX626) to $(V_{cc} - V_{ee}) < 18V$. This sets a limit to the flat-band voltage shift that can be accommodated by adjusting the amplitude of the clock pulses.

The HS S5466 CCD has identical parameters (flat-band voltage shift) as the S5466 CCD.

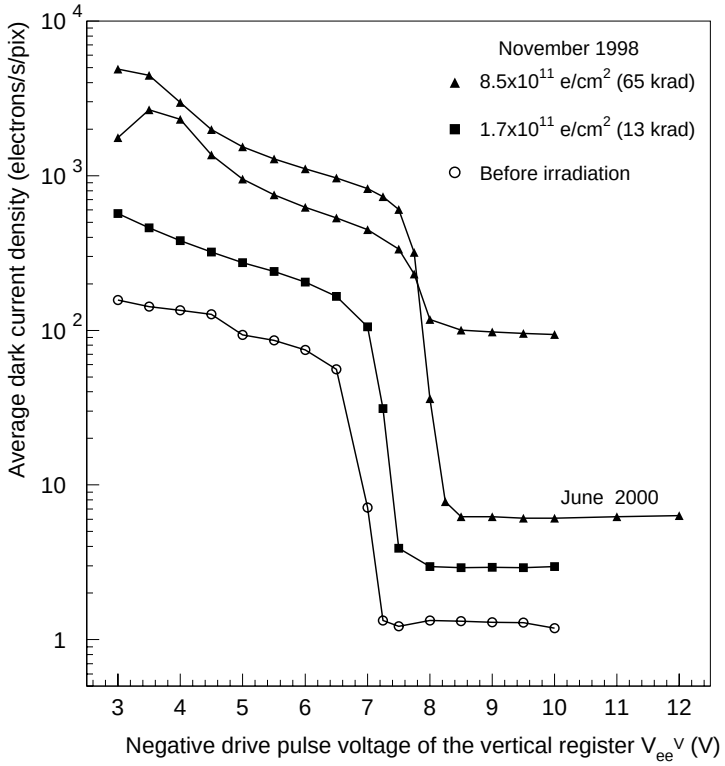

Figure 3.5: Average dark current density in EEV CCD02-06 #A4003-18 as a function of the electron irradiation fluence and of the V_{ee}^{V} at $-26°C$, $V_{ee}^{H} = -8.00$ V. The device is irradiated unbiased.

Flat band voltage shift of the EEV device (Fig. 3.5) is smaller than that in S5466 at the same irradiation level. This is attributed to the $SiO_2 - Si_3N_4$ gate dielectric, used in that CCD. The difference between the dark currents, measured immediately after the irradiation and 8 months after that is not well understood.

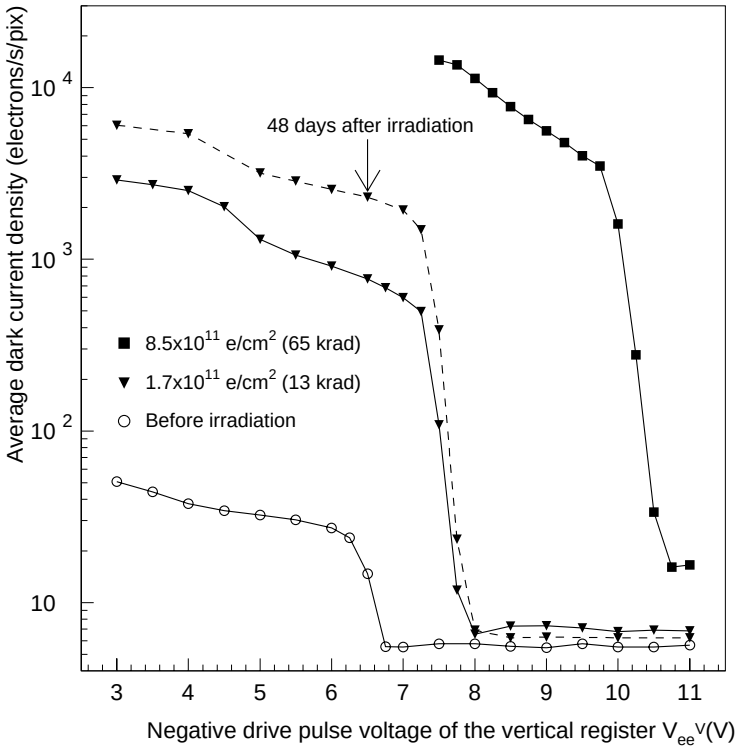

Figure 3.6: Dependence of the average dark current density on the electron irradiation fluence and on the negative drive pulse voltage $V_{\rm ee}^{\rm V}$ at -26°C, $V_{\rm ee}^{\rm H} = -8.00$ V. The device is S5466 #JS8/053, biased and clocked during irradiation.

For a device clocked under irradiation we observed significantly higher change in $\rm V_{ee}^{MPP}$, corresponding to higher flat-band voltage shift (Fig. 3.6). This result is consistent with the works of Robbins *et al.* [13] and Hopkinson [32], showing that zero bias during irradiation produces the smallest flat-band voltage shift. The flat-band voltage shift was calculated as 0.02 V/krad for unbiased devices and 0.07 V/krad for clocked CCD. The latter value is 5 times higher than that observed in radiation-hard CCD with the same oxide thickness of 100 nm [42]. The flat band voltage shifts in S5466 are slightly higher than those measured in CCDs using $SiO_2 - Si_3N_4$ dielectric system [32].

In the neutron irradiated CCDs significant flat band voltage shift was not expected,

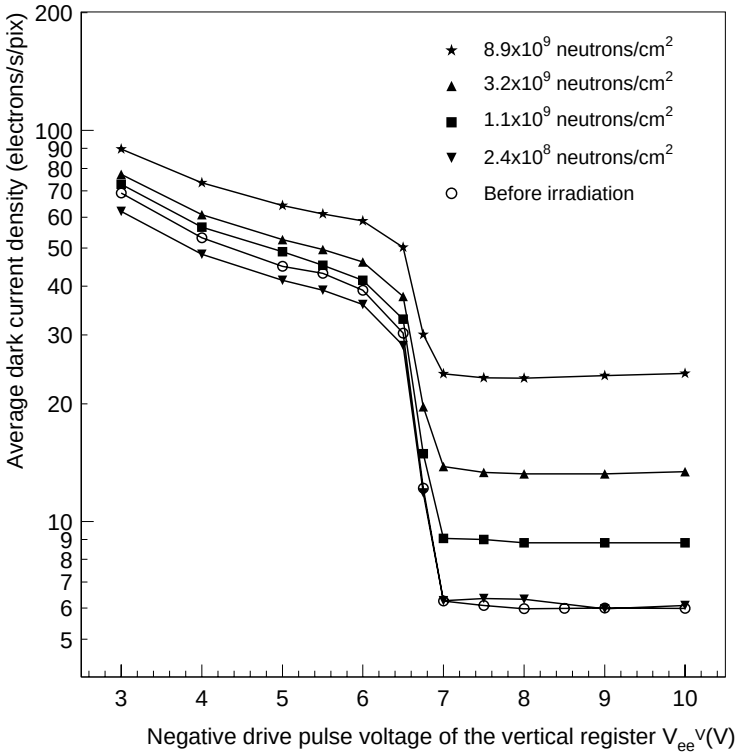

Figure 3.7: Average dark current density as a function of the neutron irradiation fluence and of the negative drive pulse voltage V_{ee}^{V} at $-26°C$, $V_{ee}^{H} = -8.00$ V (device S5466 #JS14/036).

because neutrons do not cause ionizing damage effects. However, shift can appear from the gamma background of the neutron source. The experimental data showed, that the flat band voltage shifts in those devices were too small to be observed (Figs. 3.7 and 3.8). Because of the minor ionization damage, no bias dependence of the flat band voltage shift was expected and the devices was irradiated unpowered.

3.2.2 Interface and Bulk Dark Current

At a value of $V_{ee}^{V} < V_{ee}^{MPP}$, the Si-$SiO_2$ interface is partially depleted and the dark current generation is dominated by the interface states in both non-irradiated and irradiated devices. Electron irradiation introduces defects in the interface, which increase the dark current when the device is not in MPP mode. At a value of $V_{ee}^{V} > V_{ee}^{MPP}$, the Si-$SiO_2$ interface is populated by holes and the CCD demonstrates effective suppression of the surface component of the dark current by almost 3 orders of magnitude (Figs. 3.4, 3.6).

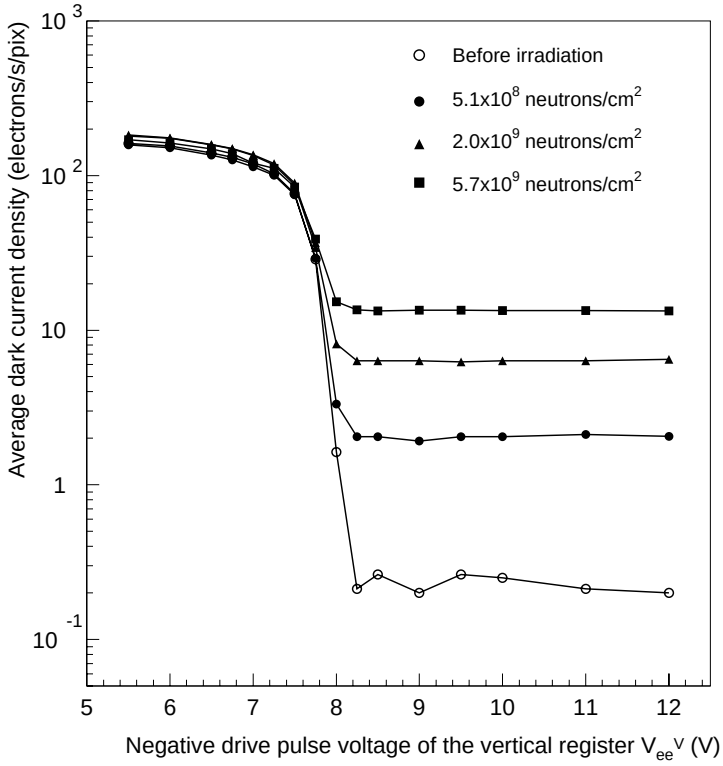

Figure 3.8: Average dark current density in EEV02-06 #A6041-48 as a function of the neutron irradiation fluence and of the V_{ee}^{V} at $-26°C$, $V_{ee}^{H} = -8.00$ V.

In that condition the dark current is limited by carrier generation in the bulk silicon, indicating that bulk damage is also present. The dark current in MPP mode in both electron and neutron irradiated devices increased after irradiation due to creation of bulk traps. In the neutron irradiated CCD the bulk damage was dominant (Fig. 3.7). Newly formed interface states due to the gamma background of the neutron source are difficult to observe, because their contribution to the dark current is smaller than the increase of the bulk generation. The dark current of an electron irradiated CCD in normal and MPP mode is given on Fig. 3.9. The ability of the MPP mode to suppress the surface component of the dark current and to extend the operating temperature range of the CCD by about 40°C is clearly demonstrated. Undamaged CCDs showed a temperature dependence of the bulk dark current of $\exp(-0.57\text{eV/kT})$, which did not change significantly after receiving a fluence of 1.7×10^{12} electrons/cm^2 or 8.9×10^9 neutrons/cm^2.

The change of the CCD gain after irradiation to $1.7{\times}10^{12}$ e$^-$/cm^2 (130 krad) was less than 2%.

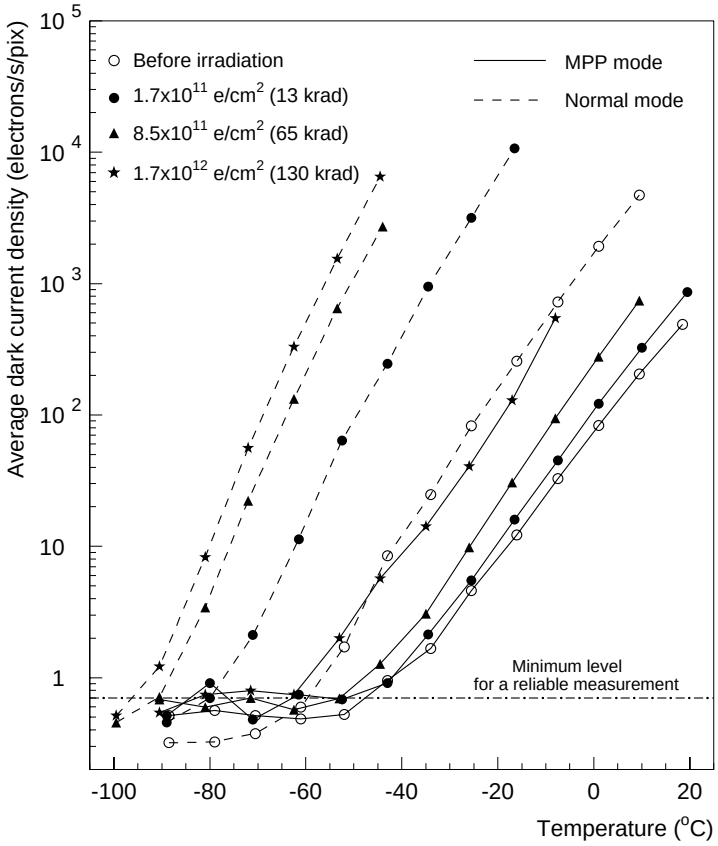

Figure 3.9: Average dark current density in device #JS14/026 as a function of the temperature and the electron irradiation fluence for MPP and normal mode of operation.

3.2.3 Spurious Dark Current

In the electron irradiated Hamamatsu CCDs an additional dark charge component, which was superimposed on the bulk current was observed. This dark charge, which can be called "dark current (or dark charge) pedestal" (DCP), was found to be generated by the charge shifting [43]. This effect is present only in Hamamatsu CCDs and was not observed in the EEV devices. All the experimental data in this subsection apply only to Hamamatsu devices.

Because the DCP does not depend on the accumulation time of the readout cycle, dark current measurements are not affected. However, the DCP provides background charge in the CCD and decreases the measured CTI through the "fat zero" effect, as will be shown in Section 4. The presence of radiation-induced DCP was unexpected and additional efforts were made to study it in detail.

In undamaged CCDs we noticed presence of spurious dark signal, which appeared at high amplitude of the clock pulses. It had a maximum value of 40 e^- at $V_{ee}^V = 11V$ in one of the samples. This current is similar to the spurious dark signal observed in virtual phase CCDs utilizing surface pinning for reduced dark current generation. Hynecek [44] explains that current by impact ionization by holes returning to the channel stops and to the adjacent gates after the surface potential has been switched from inversion to depletion. In his model the spurious current is generated on each clock and is essentially independent on the width of the clock pulses. The intensive electric fields present in the virtual phase CCDs are essential for the DCP generation.

After electron irradiation we observed large increase of the DCP in devices operated in MPP mode, while such a current was not present in the same CCDs clocked in normal mode, in which the surface is not inverted. DCP was not observed in the neutron irradiated device.

The temperature dependence of the DCP is shown on Fig. 3.10. It can be seen, that at low temperature the DCP can be several orders of magnitude higher than the bulk current, which is plotted on Fig. 3.9. The spurious dark current depends on the readout speed of the CCD through the width of the shift pulse of the vertical register. On Fig. 3.11 this dependence is plotted with the temperature serving as a parameter. At low temperature the dependence on the clock width is very close to exponential emission with time constant of approximately 10μs. The dark current pedestal exhibits also a voltage dependence on the amplitudes of the clock pulses of the vertical register. The dependencies on the values of V_{ee} and V_{cc} are shown on Fig. 3.12(a) and Fig. 3.12(b), respectively.

In the horizontal register the video level of the overclocked pixels, which is used as a reference, is sensitive to the amplitude of the clock pulses due to capacitive feedthrough to the output node and crosstalk of the gate drive current to the amplifier. Any feedthrough from the vertical shift pulses is not an issue, because it occurs during the time intervals when the horizontal register is not clocked. This variation of the level of the overclocks with the amplitude of the drive pulses masked any effect of spurious dark current in the horizontal register, and it was not possible to observe it. After electron irradiation the feedthrough effects became stronger, but the reasons for that were not well understood.

Since in electron irradiated CCDs there is significant creation of defects in the Si-SiO_2 interface, a conclusion can be drawn that the increase of the DCP is due to the newly formed interface states. The dependence of the DCP on the width of the shift

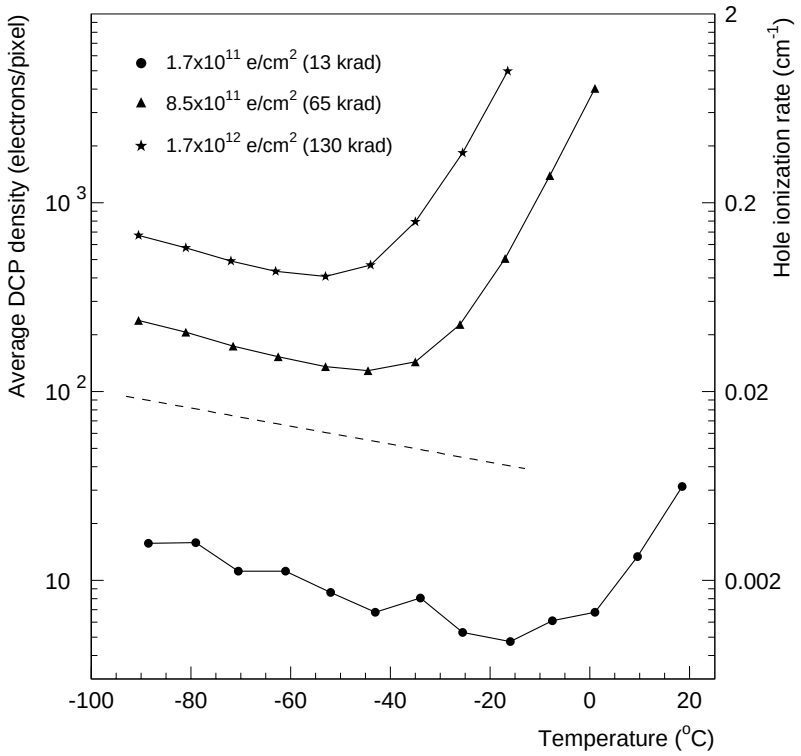

Figure 3.10: Temperature dependence of the average DCP density in device #JS14/026 for a width of the vertical shift pulse of 8μs. Measurements after irradiation to 1.7×10^{12} electrons/cm^2 were performed at $V_{ee}^{V} = -10$V and $V_{cc} = 4$V. The rest were measured at $V_{ee}^{V} = -9$V and $V_{cc} = 5$V. Dashed line shows the calculated temperature dependence of the hole ionization rate at electric field of 10^5 V/cm, based on [46].

pulse and on the temperature suggests that another mechanism beside impact ionization is involved. Therefore an extension of the model proposed by Hynecek is needed to explain the experimental results. In the low-temperature region on Fig. 3.10, the DCP decreases with increasing temperature, because the impact ionization rate is lower at higher temperatures [45][46]. Hence, the process that supplies holes for acceleration should have weak or no temperature dependence. For a qualitative comparison, the dashed line on Fig. 3.10 shows the calculated temperature dependence of the hole ionization rate, which has the form of

$$\beta = A\exp(-b/\mathcal{E}), \tag{3.4}$$

where A and b are parameters and $\mathcal{E}$ is the electric field [46]. The temperature dependence comes mainly from the parameter b, for which $db/dT = 1.1 \times 10^3$cm/V·K [46].

Because the DCP is a function of the width of the shift pulse, there must be additional

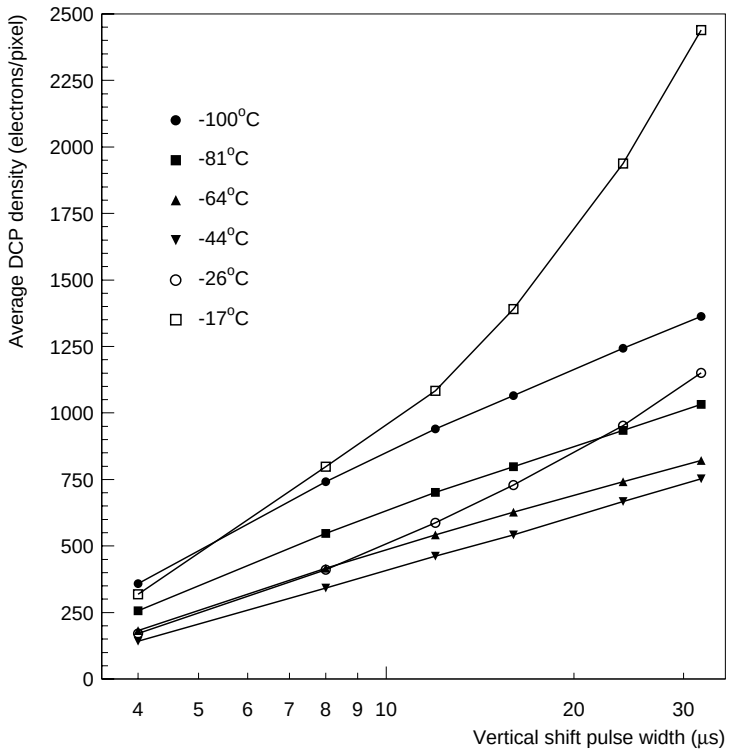

Figure 3.11: Average DCP density as a function of the width of the vertical shift pulse and of the temperature in device #JS14/026, irradiated to 8.5×10^{11} electrons/cm^2. The values of $V_{ee}^{V} = -9$V and $V_{cc} = 6$V were used during the measurement.

holes taking part in the impact ionization, beside those quickly returning to the channel stops. We suggest that in this temperature region holes are released by tunneling from near-interface defect states. Tunneling emission and injection of electrons into defects in the oxide, situated near the Si-SiO_2 interface has been observed previously [47], and it has been shown to be a temperature independent process. In the case of S5466 CCD holes are injected during inversion and then emitted by tunneling from near-interface traps in the regions between the gates, where the electric field can be higher than 10^5 V/cm. After emission, holes are accelerated by the electric field and create electron-hole pairs by impact ionization. Electrons are collected as DCP signal, as shown on Fig. 3.13. The effect occurs every time one of the phases is held at V_{ee} and the other one at V_{cc} and is therefore proportional to the number of transfers. This creation mechanism means that the closer the pixel to the horizontal register, the higher DCP charge it contains.

In the high-temperature region in Fig. 3.10 holes are emitted by thermal ionization

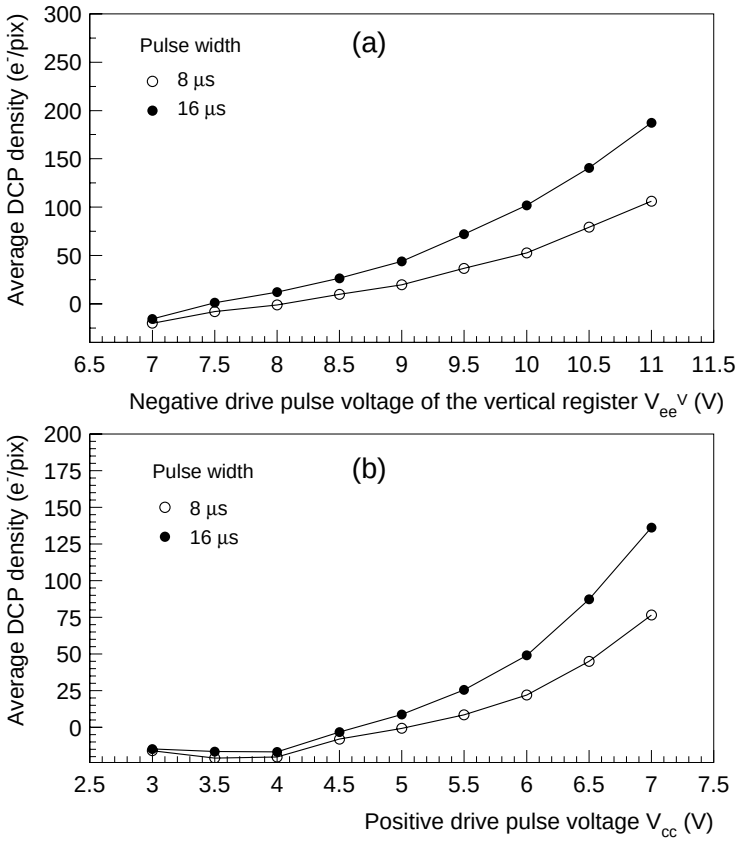

Figure 3.12: Dependence of the average DCP density on the amplitude of the vertical shift pulse for device #JS14/026, given for two different widths of the pulse and for an irradiation level of 1.7×10^{11} electrons/cm^2. The dependence on V_{ee}^{V} is measured at V_{cc} = 6V (a); the dependence on V_{cc} is for $V_{ee}^{V} = -9$V (b).

from interface states, which has an exponential temperature dependence and we observe increase of the DCP with temperature. Because interface states are distributed across the bandgap, in the high temperature region hole emission is characterized by a continuum of time constants. This is the reason we observe deviation from the exponential dependence of the DCP on the pulse width at $-26°$C and $-17°$C (Fig. 3.11).

This model qualitatively explains the observed characteristics of the DCP and its high value at low temperature. However, due to the complex structure of the CCD, quantitative model describing DCP would require measurements on simpler devices, such as test MOS capacitors in the CCD chip, which are not available at present.

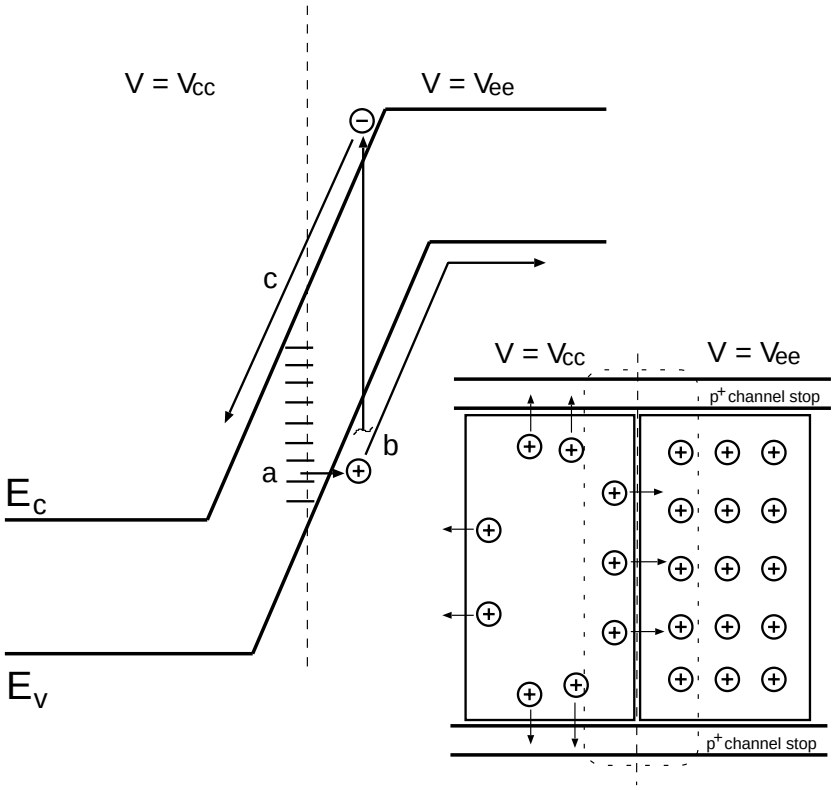

Figure 3.13: Band diagram showing the generation of DCP: (a) tunneling of holes to the valence band, (b) impact ionization and creation of electron-hole pairs, (c) electrons are collected in the potential well. The inset shows the actual movement of holes at the border between two phases.

3.2.4 Hot Pixels

Hot pixels are defined as large non-uniformities of the dark current spatial distribution in the CCD [48]. They manifest themselves as pixels with much larger dark current than the average CCD value. Those pixels can produce false signals when the CCD is used as a vertex detector.

Increase of the number of hot pixels in virtual phase CCDs, irradiated with fast protons or neutrons have been observed previously [24][49]. Their presence has been explained by the high electric fields in the devices and the radiation damage effects. In a 2-phase CCD high internal electric fields are also present, and we can expect effects similar to those observed in virtual-phase CCDs. Undamaged and electron irradiated devices did not have dark current spikes even at relatively high temperature (Fig. 3.14(a)- 3.14(d)). In the neutron irradiated CCD however, we observed significant creation of hot pixels (Fig. 3.14(e)) after irradiation with a fluence as low as 2.4×10^8 n/cm^2. After subtraction

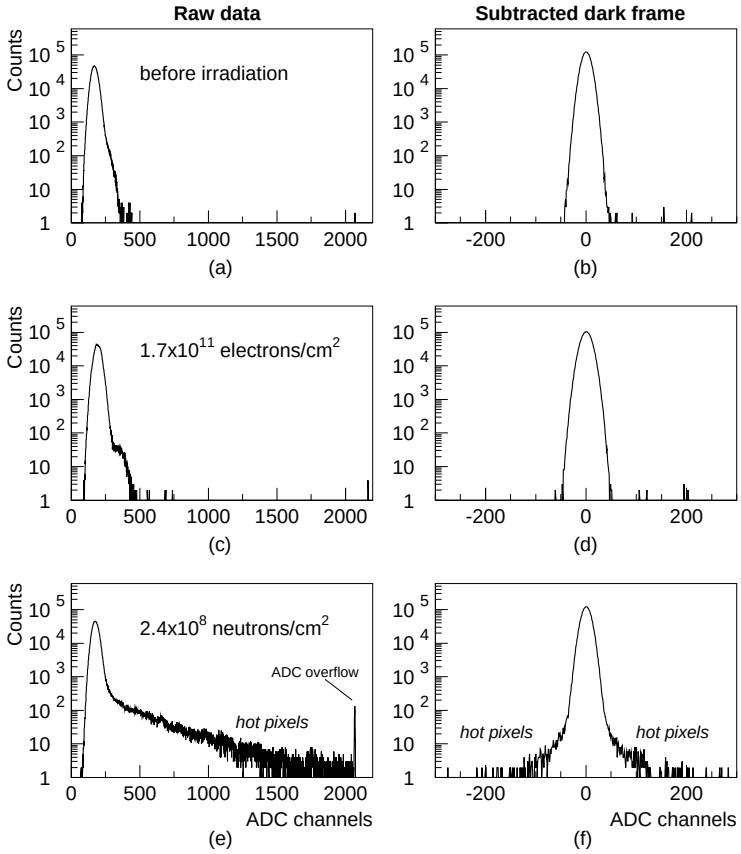

Figure 3.14: Dark current distribution at +10°C in a S5466 CCD before irradiation (a), (b) (device #JS8/053, gain = 6.0 electrons/ADC channel); in an electron irradiated to 1.7×10^{11} cm^{-2} CCD (c), (d) (device #JS8/053); and in a neutron irradiated to 2.4×10^{8} cm^{-2} CCD (e), (f) (device #JS14/036, gain = 5.8 electrons/ADC channel). The histograms are accumulated from 10 CCD frames.

of the dark frame on a pixel by pixel basis, the resulting distribution (Fig. 3.14(f)) is close to that of a electron irradiated CCD. This is an efficient way to correct for the radiation-induced dark current non-uniformity.

The dependence of the generated charge versus the accumulation time was studied in about 100 hot pixels. Deviations from the linear behaviour were not found, which implies that shorter accumulation times would lead to lower amplitude of the hot pixels. In the future vertex detector the CCDs will be read out in intervals of the order of several milliseconds and the dark current spikes are expected to be much smaller that those presented in this work. During operation, the dark current frame should be updated regularly to include the contribution of the newly created defects.

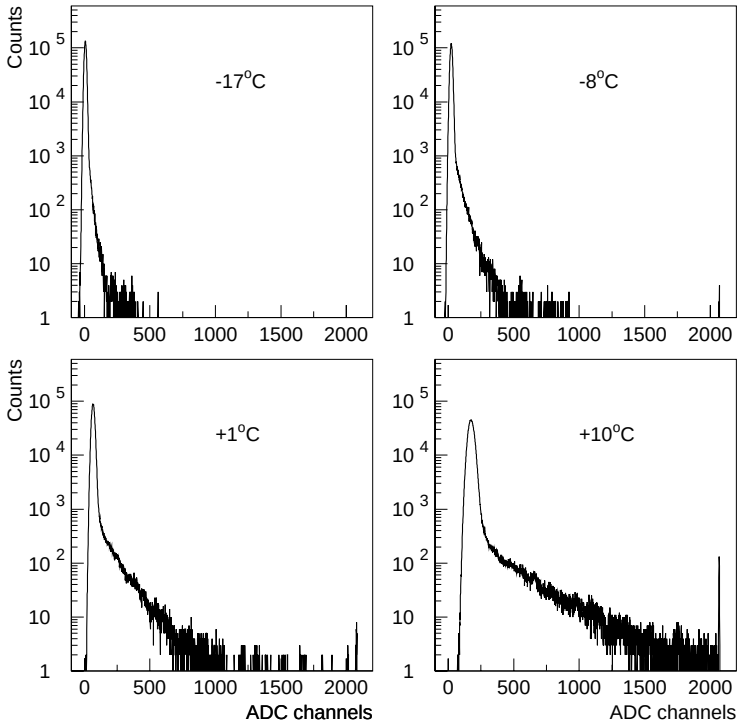

Figure 3.15: Dark current distribution at four temperatures in device #JS14/036, irradiated by neutrons to 2.4×10^8 cm^{-2}. The histograms are accumulated from 10 CCD frames.

Because some of the hot pixels contain quite large charge, the temperature range of the measurements is limited by the input range of the ADC. At lower temperatures the amplitude of dark current spikes steeply diminishes (Fig. 3.15).

To confirm the assumption that hot pixels are caused by high field phenomena, the temperature dependence of the dark current in 70 of the most intensive spikes was studied. For each pixel the dark current was plotted versus the inverse temperature and its activation energy E_a was obtained by fitting to $\exp(-E_a/kT)$. On Fig. 3.16 the dark current at -8°C is plotted versus the activation energy of each pixel. The graph shows that the most intensive spikes tend to exhibit lower activation energy. This behaviour has been attributed to field-enhanced carrier emission, such as the Poole-Frenkel effect and phonon-assisted tunneling [31][49].

The reduction of the potential barrier, caused by the Poole-Frenkel effect is given by $(e\mathcal{E}/\pi\epsilon_{Si})^{1/2}$, where $\mathcal{E}$ is the field intensity. In the channel of the S5466 CCD the vertical

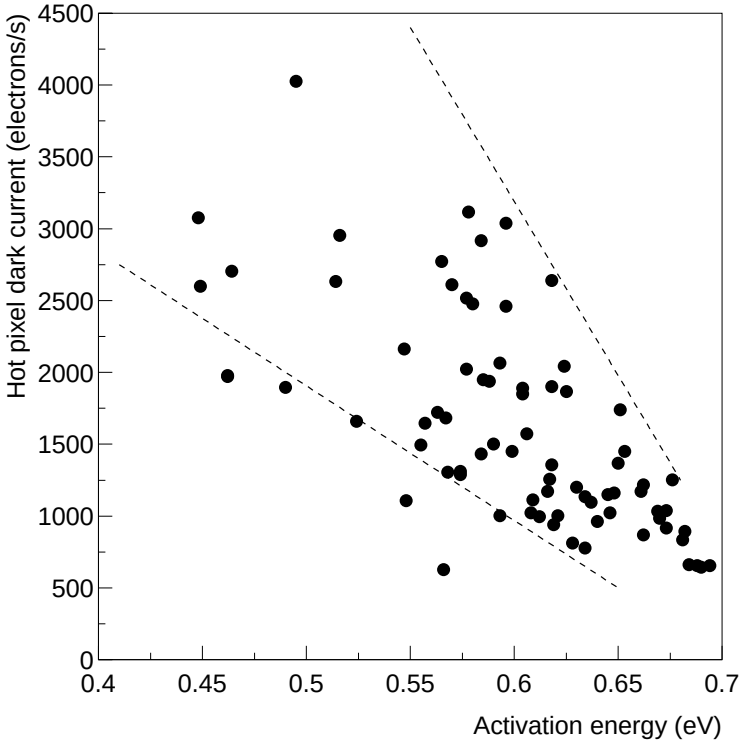

Figure 3.16: Scatter plot of the dark current versus its activation energy in the most intensive hot pixels of device #JS14/036, irradiated to 2.4×10^8 neutrons/cm^2. Dashed lines show the area where most of the points lie.

electric field has a typical value of $3{\times}10^4$ V/cm, which is much stronger than the horizontal fringing fields. Using the above mentioned field intensity to calculate the lowering of the potential barrier, we get a value of 0.04 eV. Since the majority of the hot pixels on Fig. 3.16 have an activation energy of around 0.60 eV, it can be concluded that the energy reduction for most of the defects is not higher than the obtained value. However, some of the hot pixels on Fig. 3.16 show much stronger reduction of their activation energy, in the order of 0.15 eV. Probably these dark current spikes are caused by defects, situated near the Si-SiO_2 interface, where the field is stronger than 10^5 V/cm. It is likely that the phonon-assisted tunneling, which causes larger enhancement [49], plays a role in those hot pixels. It must be noted, that the same reduction of E_a should apply not only to traps, close to the mid-gap level and responsible for the dark current generation, but also to shallower defects.

Random Telegraph Signals

Further experiments were carried out to study the time dependence ot the dark current, generated in the hot pixels. It is known, that in proton and neutron irradiated CCDs the dark current in some hot pixels is not stable, but changes with time [32]. The time dependence is random, with transitions between 2 or more levels, and it is similar to the Random Telegraph Signals (RTS), observed in MOS transistors and other devices. Hopkins *et al.* [34] [35] has conducted detailed studies on RTS in CCDs, which have revealed the following:

1) The higher the amplitude of the hot pixel, the higher the probability it shows RTS behavior;

2) The RTS amplitude and the average dark current level are not correlated, i.e. there are some pixels with relatively small dark current, but with high RTS amplitudes, as well as intensive hot pixels with small RTS signals;

3) Time constants of the RTS signals (the average time in "high" and "low" states) have exponential temperature dependence. However, there are a number of hot pixels, which show anomalous behavior, such as fast switching at low temperature or sudden change of the RTS amplitude or the time constant;

4) The RTS are caused by bulk defects, and are not affected by the surface potential of the CCD;

5) There is evidence that the RTS generation is connected to field-enhanced emission from defects.

The RTS nature has been explained by presence of bistable effects in the disordered regions, generated by heavy particles. RTS has also been observed in nonirradiated devices, which has been attributed to dislocations and stacking faults. In the short time scale, needed for one CTI measurement (typically $\approx$5 minutes), the RTS signals are difficult to notice, because of the long time constants of the transitions [35]. However, if the dark current is recorded for a time of the order of hours, RTS are easy to observe. The signals they create can be falsely attributed to particles, traversing the CCD, and can be a source of erroneous track reconstruction.

Figures 3.17 and 3.18 show RTS behaviour of the dark current in several hot pixels

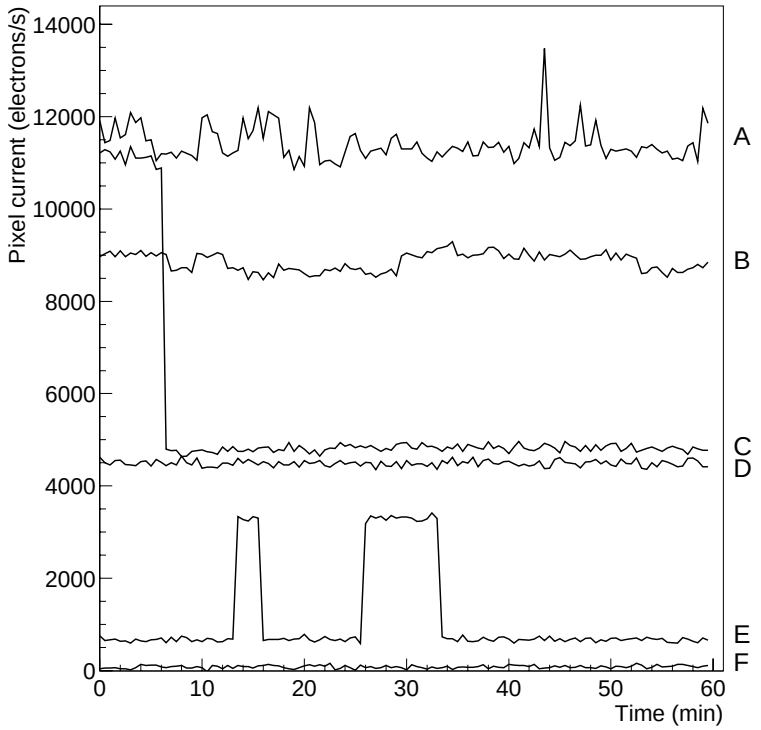

Figure 3.17: Time variation of the dark current at -1.6°C in hot pixels, showing RTS behavior. The measurement was carried out on Notch CCD #P4 1-5B1-4, irradiated to 5.7×10^9 neutrons/cm^2. Pixel F is normal (not "hot") and is plotted for reference.

of a neutron-irradiated CCD. There are several distinguishable patterns, which can be summarized as follows:

1) Pixels with high amplitude of the RTS signal, which show transitions between more than 2 states (A, G, J);

2) RTS in the form of step-like transitions between 2 states (C, E, K);

3) Pixels with excessive noise, but without visible RTS signal ("noisy RTS") (H);

4) Relatively smooth change of the dark current ("smooth RTS") (B, I);

5) Pixels with high dark current, but without RTS (D).

Pixel E shows high transition amplitude on low pedestal, whereas pixel G has smaller amplitude on higher mean dark current. Figure 3.19 shows the increase of the switching time constant with temperature in a Hamamatsu device. Measurements on neutron-irradiated EEV CCD revealed very similar picture of the time and temperature depen-

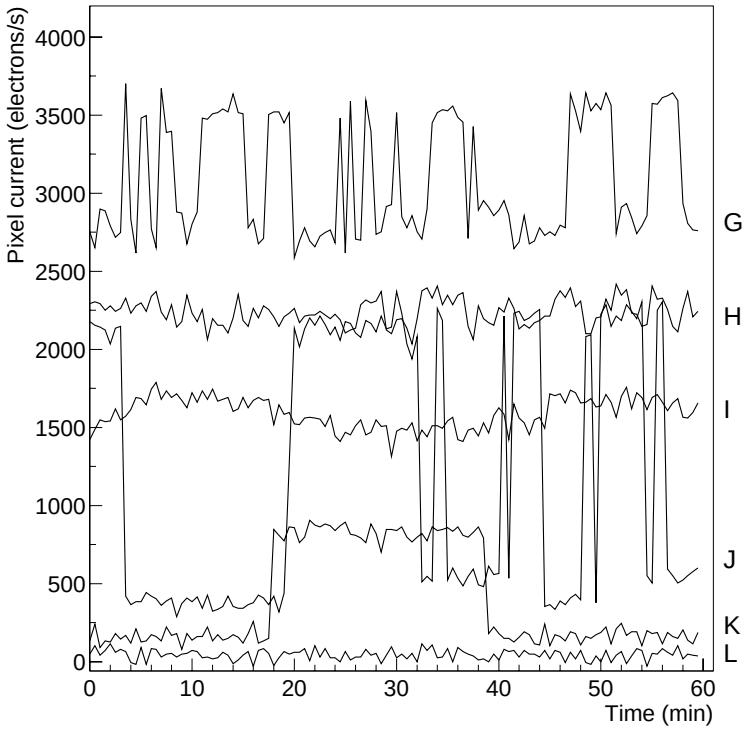

Figure 3.18: Time variation of the dark current at -1.6°C in hot pixels, showing RTS behavior. The measurement was carried out on Notch CCD #P4 1-5B1-4, irradiated to 5.7×10^9 neutrons/cm^2. Pixel L is normal (not "hot") and is plotted for reference.

dence of the RTS. It should be noted, that there were several pixels in the investigated EEV CCD, that showed RTS behavior even *before* irradiation.

Taking into account the measurements presented above, one can try to estimate the number of RTS hot pixels, which can be erroneously taken for signal from MIPs in a realistic environment. Such a measurement was carried out on a neutron-irradiated Notch CCD. The rate of false IPE events, caused by RTS was used as a measure of the false events, expected in a vertex application. The experimental procedure for finding false IPE was the same as those used in the CTE measurements and described in Subsection 3.1.3.

If the CCD is read periodically for a long time, one can observe that RTS from certain pixels deviate from the average dark current, recorded just before the mesurement. These signals create signals, undistinguishable from those, generated by X-rays, however the number of false IPE greatly depends on the threshold, which is imposed for the search of signal. The same threshold of 600 electrons, used in the CTI measurements was applied

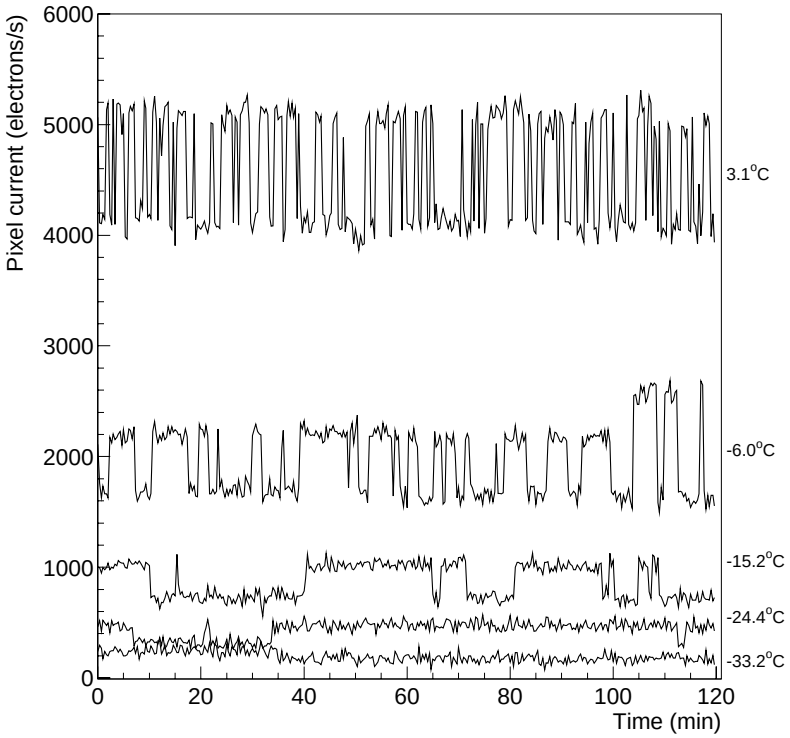

Figure 3.19: RTS in a hot pixel at different temperatures. It can be noticed, that the frequency of the transitions, as well as the mean dark current increase with the temperature. At -6.0°C the defect changes the amplitude of its transitions. The measurement was carried out on Notch CCD #P4 1-5B1-4, irradiated to 5.7×10^9 neutrons/cm^2.

for the search of false IPE. The ratio of false IPE per CCD readout frame (i.e. pixel occupancy), caused by RTS is shown on Fig. 3.20. As the amplitude of the RTS depends on the temperature and the integration time t_i, these 2 parametes were varied during the measurement.

Because the dark current map is recorded at an arbitrary moment, the reference value of the RTS pixels can happen to be either their "low" or "high" state. If the reference is in the "low" state, then further transitions cause isolated pixel events; if it is in the "high" state, those pixels apparently do not cause IPE. Because they are potentially a source of IPE, their contribution should also be considered. This was done by taking the absolute value of the difference of the dark current map and the pixel readout value.

Futher measurement was performed in order to estimate how many of the total number of hot pixels can generate RTS. As was mentioned above, the number of false IPE depends

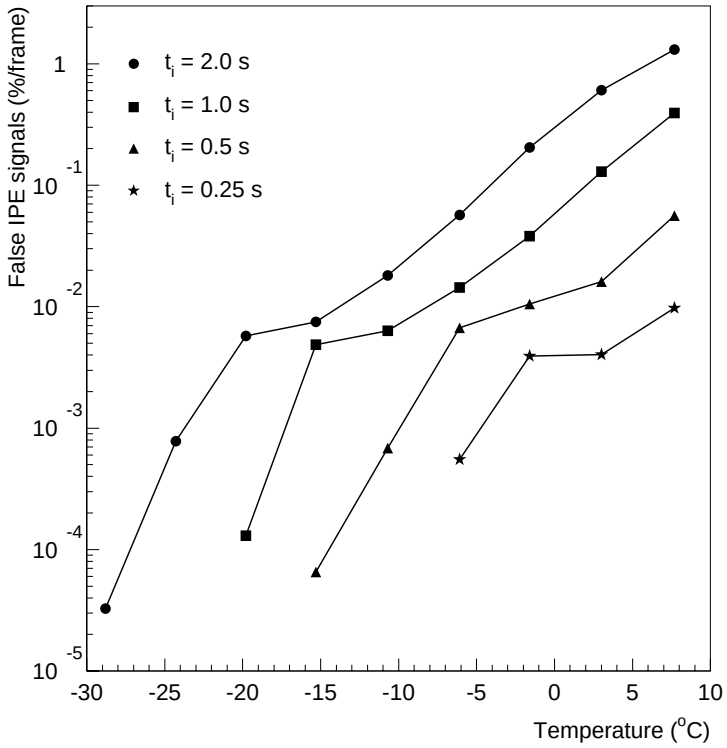

Figure 3.20: Ratio of false IPE per CCD frame, caused by RTS, at 4 different integration times t_i. The measurement was performed on Notch CCD #P4 1-5B1-4, irradiated to 5.7×10^9 neutrons/cm^2. The threshold is set at 600 electrons.

on the temperature, integration time and applied threshold. This measurement requires that the term "hot pixel" is defined more precisely.

Usually, a pixel is considered as being "hot" when its dark current is significantly higher than the average CCD dark current. For device application however, dark current of each pixel is seldom measured and some additional considerations can be appropriate. At sufficiently low temperature or fast readout, the charge in the hot pixels can become so small, so that it is hidden in the noise. Therefore, for a practical definition of the term "hot pixel", both the dark current and the readout noise should be taken into account. One definition could be, that a pixel should contain charge above the threshold

$$Q_{HP}^{th} = Q_{dark}^{CCD} + 5 \times \sigma_{dark}, \tag{3.5}$$

where Q_{dark}^{CCD} is the average pixel charge, to be considered "hotter" than the rest of the pixels. Obviously, the number of hot pixels, which have charge greater than Q_{HP}^{th} depends on the temperature, the CCD integration time t_i and the noise.

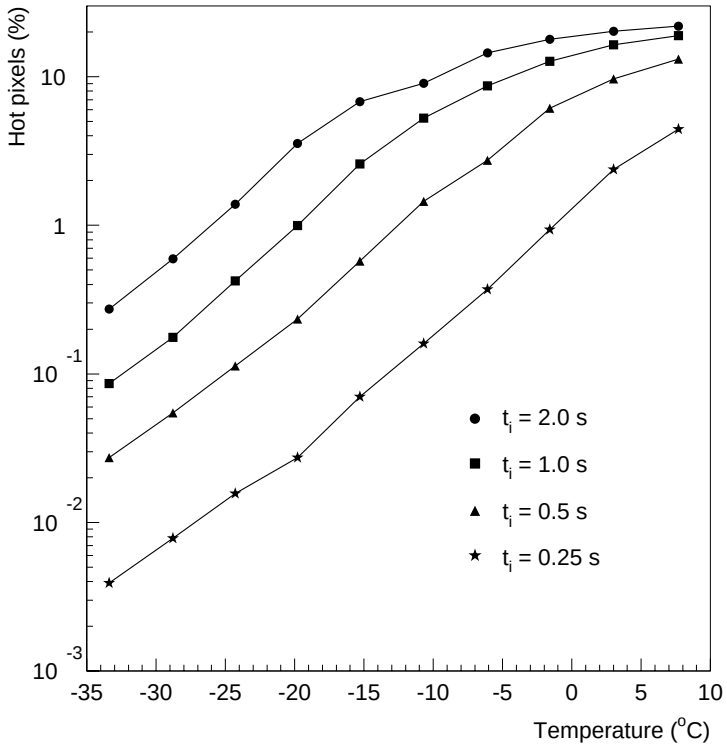

Figure 3.21: Ratio of hot pixels, calculated according to (3.5) in Notch CCD #P4 1-5B1-4, irradiated to 5.7×10^9 neutrons/cm^2.

Figure 3.21 shows the number of pixels above Q_{HP}^{th}, expressed as a ratio of the total CCD pixel number, as a function of the integration time and the temperature. By comparing Fig. 3.20 and Fig. 3.21 one can conclude, that even in the worst case less than 10% of the hot pixels cause false IPE. Although about 40% of the hot pixels exhibit RTS signals, most of them are rejected by the applied threshold for IPE. When the integration time is short, a ratio of false IPE signals of less than 10^{-4} can be achieved even in the temperature range above 0°C.

As will be shown later in Chapter 4, the CTI, caused by the expected neutron irradiation (of the order of 5×10^9 neutrons/cm^2) is much smaller than the electron-induced CTI. The main effect, caused by neutron irradiation is creation of hot pixels and their time fluctuations. Measurements have shown, that the pixel occupancy, caused by RTS is below 10^{-4} at integration time of 250 ms and temperature around 0°C. The considerations on IPE generation by RTS and Fig. 3.20 indicate that with faster readout the occupancy can be even smaller.

Chapter 4

Charge Transfer Model and CTI Measurements

4.1 Theory of Charge Trapping

In a buried channel CCD charge is transported far from the defect states at the Si-SiO_2 interface and only the interaction of the signal packets with the bulk traps needs consideration. In the presence of bulk defects electrons can be trapped with a capture time constant of τ_c and consequently released with an emission time constant of τ_e. For a defect at energy position E_t below the conduction band the Shockley-Read-Hall theory gives

$$\tau_e = \frac{1}{\sigma_n X_n v_{th} N_c} \exp\left(\frac{E_t}{kT}\right) \tag{4.1}$$

and

$$\tau_c = \frac{1}{\sigma_n v_{th} n_s}, \tag{4.2}$$

where

σ_n = electron capture cross section;
X_n = entropy change factor by electron emission;
v_{th} = thermal velocity for electrons;
N_c = density of states in the conduction band;
k = Boltzmann's constant;
T = absolute temperature;
n_s = density of signal charge.

Charge losses occur when defects capture electrons and emit them at a later moment, so that the released charge cannot join the original signal packet from which it has been

trapped. Since the charge is transferred within several nanoseconds to the next pixel by the fringing fields, the trapping during the transfer time can be neglected. We consider effects of trapping and emission solely during the charge dwell time.

At low temperature, the emission time constant of the defects can be very large, of the order of seconds (Table 4.1). The capture time constant has weaker temperature dependence and it is in the order of several hundred nanoseconds. Once a defect has captured an electron (which can be generated by ionization or thermally), the trap remains occupied for a time, much longer than the charge shift time, which is in the order of microseconds. Therefore, the defects cannot capture electrons and the CTI at low temperature is small. At high temperature, the emission time constant becomes small and comparable with the charge shift time. Trapped electrons are able to join their signal packet, because most of them are emitted already during the shift, and the CTI is small. At temperatures between these two extremes there is a peak in the CTI value.

Table 4.1: Emission τ_e and capture τ_c time constant of the $V-V^-$ and $P-V$ defects at several temperatures. The signal is $1620e^-$ in a well with size of $24 \times 6 \times 0.15$ μm^3. The defect parameters are taken from Table 4.2.

T, °C	$V-V^-$		$P-V$	
	τ_e	τ_c	τ_e	τ_c
−100	589 ms	266 ns	5.9 s	354 ns
−80	32 ms	252 ns	255 ms	335 ns
−60	2.86 ms	240 ns	19.5 ms	319 ns
−40	386 μs	229 ns	2.3 ms	305 ns
−20	70 μs	220 ns	372 μs	293 ns
0	16.3 μs	212 ns	78 μs	282 ns
10	8.5 μs	208 ns	38.5 μs	277 ns

There are several commonly observed defects in electron or neutron irradiated n-type silicon, listed in Table 2.1. For near-room temperature application we can consider only defects that are known to cause noticeable CTI in that temperature range [13][50]. Such traps are the $E-$center and the divacancy ($V-V^-$). Another defect at $E_c-0.30$ eV with an unknown nature has also been observed [26][27], with a creation rate several times smaller than that of the $V-V^-$ and $E-$centers.

Table 4.2 gives the parameters of the three traps, which are used for the CTI model calculations. The parameters are within the range commonly found in the literature data.

Table 4.2: Parameters of the traps of interest.

Defect	$E_c - E_t$, eV	σ_n, cm^2	Reference
$P-V$	0.42	3×10^{-15}	[24]-[26]
$V-V^-$	0.39	4×10^{-15}	[27]
unknown	0.30	5×10^{-15}	[26, 27]

Following the approach of A. Holland [26], the charge storage volume in the Hamamatsu S5466 CCD was estimated to be $24 \times 6 \times 0.15$ μm^3. It should be noted, that this is an approximation and in reality the charge packet does not have sharp edges. This volume is considered constant for charge packets smaller than few thousand electrons.

4.2 Charge Transfer Model for 2-phase CCD

4.2.1 CTI Model for the Horizontal Register

In the horizontal register charge is transferred by applying square wave pulses, shifted by 180°, to the gates P1 and P2 (Fig. 4.1). Because the S5466 CCD utilizes p-type implant to form the potential barriers for charge separation within one pixel, electrons are stored in the potential wells under the part of the gate structure next to the implant. We apply the Shockley-Read-Hall theory to the potential well in the storage region under the phase P1. We consider the case of a charge packet transported along the horizontal register at a distance of m pixels from the previous signal packet.

CTI is studied by calculating the ratio of filled traps [52], defined as $r_f = n_f/N_t$, where n_f is the concentration of the defects, that have captured an electron, and N_t is the defect concentration. Let us suppose that at the moment A the traps in the region have an occupancy of r_f^A. After the voltages applied to P1 and P2 reverse their values, the defects start to emit their trapped charge and the ratio of filled traps at the moment B becomes

$$r_f^B = r_f^A \exp(-t_w^H/\tau_e), \tag{4.3}$$

where t_w^H is the width of the horizontal shift pulse. When the signal packet arrives to the region, the concentration of filled traps n_f under P1 and the occupancy r_f^C at the moment C can be found by solving the equation

$$\frac{dn_f}{dt} = \frac{N_t - n_f}{\tau_c} - \frac{n_f}{\tau_e}, \tag{4.4}$$

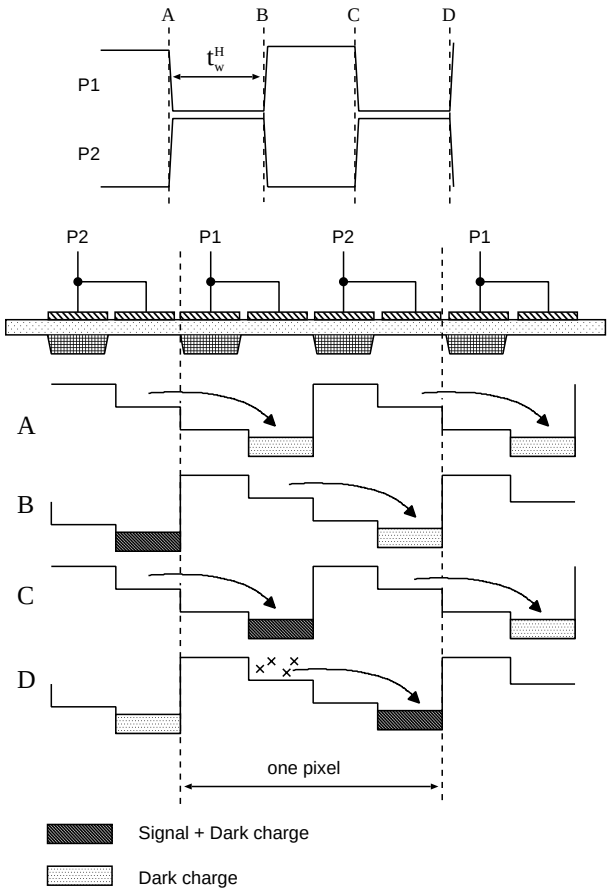

Figure 4.1: Typical clock sequence and a diagram of the consecutive transfer stages in the horizontal register of the S5466 CCD.

with an initial condition of $n_f/N_t = r_f^B$, and τ_c determined from the concentration of signal charge n_s (4.2). Provided that $n_s \gg N_t$, the solution is

$$r_f^C = \left(r_f^B - \frac{\tau_e}{\tau_e + \tau_c}\right) \exp\left\{-t_w^H \left(\frac{1}{\tau_e} + \frac{1}{\tau_c}\right)\right\} + \frac{\tau_e}{\tau_e + \tau_c}. \tag{4.5}$$

This result holds for the general case where full occupation of the traps in the presence of signal charge is not assumed. For very low values of n_s however, τ_c becomes a function of the trap occupation and cannot be considered a constant. This usually corresponds to the case of transporting very small charge or the dark current alone. In that condition (4.5) is no longer valid and r_f^C is obtained by solving the equation (4.4) numerically:

$$\frac{dr_f}{dt} = (1 - r_f)\sigma_n v_{th} n_s - \frac{r_f}{\tau_e}. \tag{4.6}$$

Here n_s accounts for the concentration of the signal charge and any electrons, released or captured by the defects during the charge dwell time.

After the charge has been shifted to the region under P2, the ratio of filled traps at the moment D becomes

$$r_f^D = r_f^C \exp(-t_w^H/\tau_e). \tag{4.7}$$

The charge loss in the region under P1 is proportional to the difference between r_f^D and r_f^B. Because the phases P1 and P2 are equivalent, the horizontal CTI per pixel is given by

$$HCTI = 2\,\frac{N_t}{n_s}(r_f^D - r_f^B). \tag{4.8}$$

The occupancy r_f^A can be found by applying (4.3)-(4.5) m times, starting with an initial condition of $r_f^A = 1$, and using $n_s = n_{dark}$. The initial condition follows from the assumption, that the signal charge usually contains large number of electrons, which can fully occupy all the traps in the storage area. In this way one can simulate the effect of the density of the X-ray events on the CTI. It is also possible to investigate the effect of the background charge on the CTI by varying the value of n_{dark}.

4.2.2 CTI Model for the Vertical Register

The charge transfer in the vertical register has to be considered separately for the regions under P1 and P2 because of the different time the charge packet spends under the two halves of the pixel. The clock sequence used for the charge transfer and the diagram of the consecutive transfer stages are given on Fig. 4.2. Charge is stored entirely under P2 during the horizontal shift time, which affects to a great extent the CTI, caused by that region.

For the well under P1 two transfer steps have to be considered: (a) transfer of charge from the previous pixel (A-B); and (b) charge transfer to P2 of the same pixel and emission of trapped electrons (B-C). The filling ratios are obtained from (4.3) and (4.5) using t_w^V for the width of the shift pulse. Supposing that the initial trap occupation under P1 is $r_f^A(\mathrm{P1})$, the CTI for that region is

$$CTI(P1) = \frac{N_t}{n_s}\{r_f^C(P1) - r_f^A(P1)\}. \tag{4.9}$$

There are 3 transfer steps for the region under P2: (a) electron emission (A-B); (b) the charge transferred from P1 stays under P2 for the period of t_w^V plus the horizontal shift time (B-C-D); and (c) charge transfer to the next pixel and emission of trapped electrons

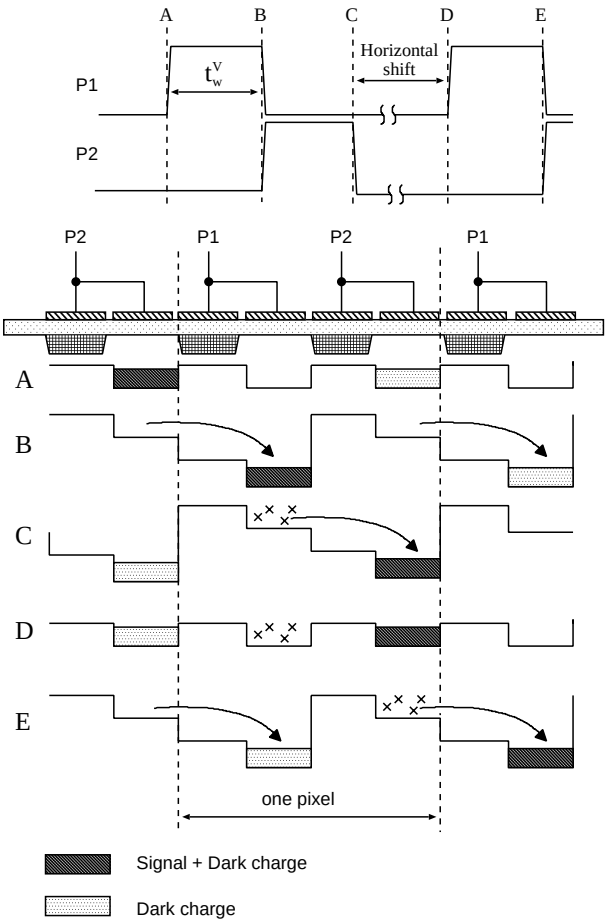

Figure 4.2: Typical clock sequence and a diagram of the consecutive transfer stages in the vertical register of the S5466 CCD.

(D-E). For the region under P2 the CTI is

$$CTI(P2) = \frac{N_t}{n_s}\{r_f^E(P2) - r_f^B(P2)\}. \tag{4.10}$$

The filling ratios for the steps (a) and (c) are obtained from (4.3) using t_w^V for the width of the shift pulse. For the step (b) the filling ratio is calculated from (4.5) using for the width of the shift pulse the value $t_w^V + 2{\times}t_w^H \times hpix$, where $hpix$ is the number of pixels in the horizontal register. The CTI per pixel of the vertical register is then given by

$$VCTI = CTI(P1) + CTI(P2). \tag{4.11}$$

The initial occupancies r_f^A(P1) and r_f^A(P2) can be found in the same way as those used for the horizontal register.

It is important to study the dependence of the CTI on the concentration of background and signal charges, because it affects significantly the experimentally determined CTI val-

ues [50]. For near-room temperature operation the dark current, which has an exponential temperature dependence, should be considered even for MPP devices. Additional source of background charge can be the dark current pedestal, described in Section 3.2.3, or an artificially introduced charge through the input structure of the CCD. In a vertex detector a MIP produces about 1080 electrons in a 10μm thick epitaxial Si layer [51], so that we can assume that the charge created in each pixel contains approximately the same number of electrons. Under these considerations, we study only the dependence of CTI on the background charge; and to be able to compare with the experimental data the signal charge is taken to be 1620 electrons.

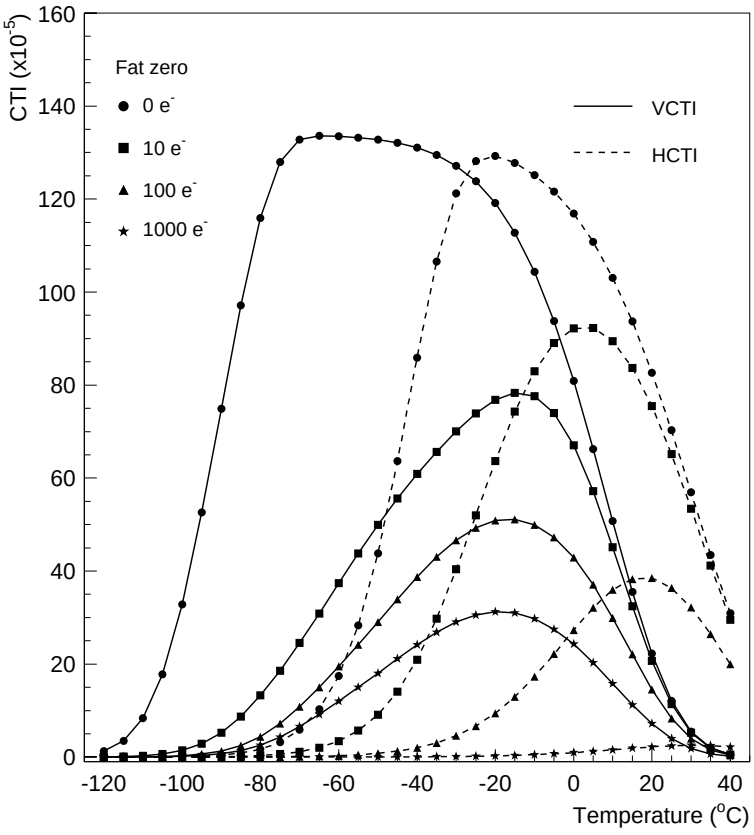

Figure 4.3: Modeled HCTI and VCTI as a function of the temperature and of the background charge, with a concentration of the $V - V^-$ center of 5×10^{10} cm^{-3}. Widths of the clock pulses are $t_w^H = 2\mu$s and $t_w^V = 8\mu$s.

On Fig. 4.3 the modeled HCTI and VCTI are plotted as a function of the temperature and the number of the fat zero electrons for the $V - V^-$ center with parameters listed in Table 4.2. The values of $X_n = 2$ and $v_{th}N_c = 1.6 \times 10^{21}\ T^2$ cm^{-2}s^{-1} were used in

the calculation. The widths of the vertical and the horizontal shift pulses are typical to the values used in the experiment. Fig. 4.3 shows that even small background charge can decrease significantly the CTI. The peak of the VCTI occurs at lower temperature than the peak of the HCTI because $t_w^V > t_w^H$. It is seen that a significant reduction of the HCTI can be achieved in the temperature range from -40 to $+20$°C by introducing fat zero charge. The VCTI also decreases in the presence of background charge, but the effect is relatively smaller than that on the HCTI. Due to the different time the charge spends in the regions under P1 and P2 of the pixels in the vertical register, the behavior of the VCTI as a function of the background charge differs from that of the HCTI.

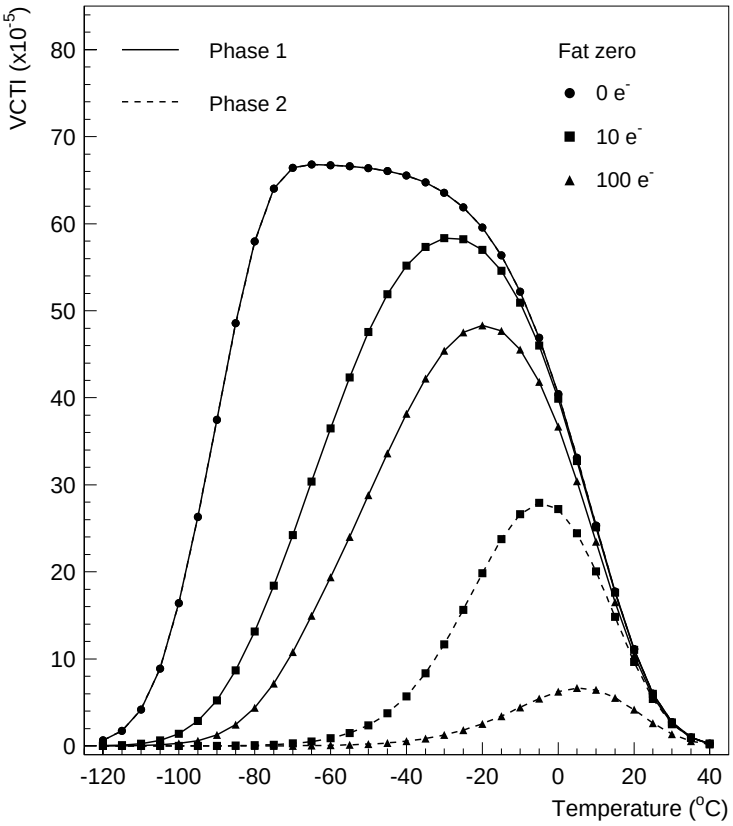

Figure 4.4: Modeled VCTI as a function of the temperature and of the background charge in the regions under P1 and P2 of the vertical register. Concentration of the $V - V^-$ center is $5{\times}10^{10}$ cm^{-3}. Widths of the clock pulses are $t_w^H = 2\mu$s and $t_w^V = 8\mu$s. The curves for zero background current coincide.

The simulation on Fig. 4.4 shows that the region under P1 is the main source of VCTI in the presence of background charge. The model shows, that the reason for this behavior

is that the traps in the region under P1 have enough time to become empty during the horizontal shift time. When the signal packet arrives to P1, trap occupation is low and almost all of them can capture electrons. The signal comes under P2 shortly after the dark charge has left the region, trap occupation is still high and less electrons can be captured. From Fig. 4.4 it is seen that the CTI caused by region under P1 is less sensitive to the presence of background charge than the region under P2. Because of this feature, introducing fat zero charge has smaller effect on the VCTI, than on the HCTI.

4.3 Charge Transfer Model for 3-phase CCD

The charge transfer model for 3-phase CCD was built using the method developed for 2-phase CCD [52]-[54] and considering the model proposed by Hardy *et al.* [55].

4.3.1 CTI Model for the Horizontal Register

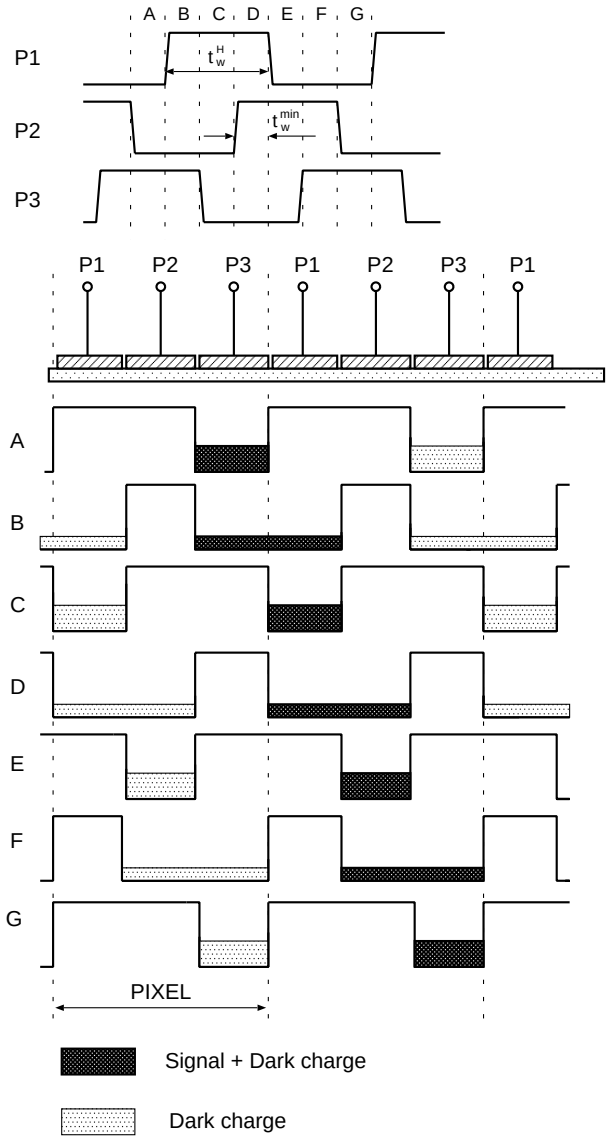

Figure 4.5: Clock sequence and a diagram of the consecutive transfer stages in the horizontal register of a 3-phase CCD.

Let us consider the region under the phase P1 in a 3-phase CCD (Fig. 4.5). An appropriate time unit for the following considerations is the width of the overlapping of

the clock pulses t_w^{min}. The horizontal clocks are symmetrical with width $t_w^H = 3\ t_w^{min}$. It should be noted, that another clock sequence, in which the pulses overlap at their 50% points is also possible.

At the beginning of the time period B the signal charge arrives under P1 shared with P3. The evolution of the trap filling ratio r_f can be found by applying the equation (4.5) three times for each of the intervals B, C and D. Calculation of r_f^B requires that the filling ratio r_f^A at the end of the period A is known, which we will assume. In the time intervals B and D the signal density is 2 times lower than the density during C because of the charge sharing with the P3 and P2, and this is taken into account for the calculation of τ_c. The charge dwell time for the periods $B - D$ is t_w^{min}. The charge leaves the region under P1 at the beginning of the period E and the traps emit trapped electrons during the time $E - G$. The ratio of filled traps at the end of the period G is

$$r_f^G = r_f^D\ \exp(-t_w^H/\tau_e). \tag{4.12}$$

Analogously with (4.8), the HCTI per pixel becomes

$$HCTI = 3\ \frac{N_t}{n_s}(r_f^G - r_f^A) \tag{4.13}$$

because all the three phases are equivalent.

The initial occupancy r_f^A can be found in the same way as described for the 2-phase CCD: start with $r_f^A = 1$ and repeat the transfer on Fig. 4.5 m times, using $n_s = n_{dark}$. For very small dark charges, corresponding to $n_s \sim N_t$, the solution of (4.4) is obtained numerically as in (4.6).

4.3.2 CTI Model for the Vertical Register

The charge transfer model for the vertical register is more complicated than for the horizontal one because of the three time intervals, which have to be considered. These are the clock width t_w^V, the overlapping t_w^{min} and the horizontal shift time $t_{shift}^H = 2 \times t_w^H \times hpix$ (Fig. 4.6). As for the 2-phase CCD, the regions under the three phases have to be studied separately because of the different time charge spends under them.

The transfer cycle starts with the end of the integration period, during which all the phases are equally biased. The charge is collected and stored under P2 and P3, because the phase P1 is the MPP gate. At the end of the horizontal shift time the region under

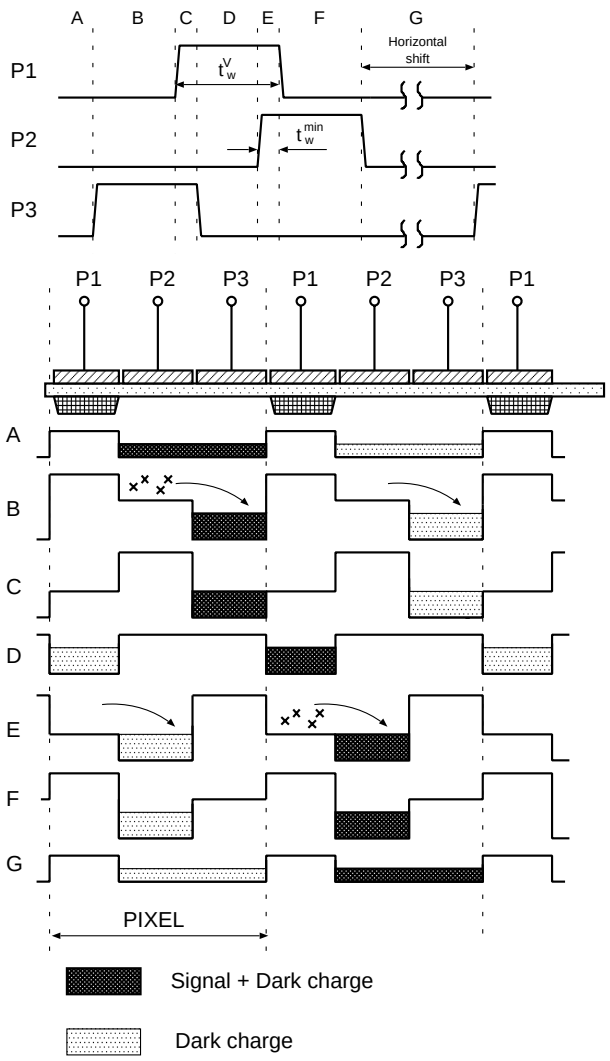

Figure 4.6: Clock sequence and a diagram of the consecutive transfer stages in the vertical register of a MPP mode 3-phase CCD.

the phase P1 has an occupation of $r_f^A(P1)$, and the filling ratios for the phases P2 and P3 are equal:

$$r_f^A(P2) = r_f^A(P3). \tag{4.14}$$

The signal charge arrives under P1 after the traps have emitted during the periods B and C, and the filling ratio at the end of C is

$$r_f^C(P1) = r_f^A(P1)\,\exp(-t_w^V/\tau_e). \tag{4.15}$$

Signal electrons stay under P1 during the period D, and the filling ratio $r_f^D(P1)$ at the end can be found from (4.5), using $(t_w^V - 2 \times t_w^{min})$ for the dwell time and $r_f^C(P1)$ for the initial trap occupation. The charge is transferred to P2 at the beginning of the period E

and trapped electrons can be emitted into their signal packet during that time. The ratio $r_f^E(P1)$ is

$$r_f^E(P1) = r_f^D(P1)\ \exp(-t_w^{min}/\tau_e), \tag{4.16}$$

and the CTI, caused by the phase P1 can be expressed as

$$CTI(P1) = \frac{N_t}{n_s}\{r_f^E(P1) - r_f^C(P1)\}. \tag{4.17}$$

The transfer cycle for the phase P2 has the feature, that the charge is shared with P3 during the horizontal shift time. The signal comes to P2 after the traps have emitted during the interval $B-C-D$, therefore at the end of the period D the filling ratio under P2 is

$$r_f^D(P2) = r_f^A(P2)\ \exp\{-2\ (t_w^V - t_w^{min})/\tau_e\}. \tag{4.18}$$

The signal charge arrives under P2 at the beginning of the period E and stays there during the interval $E-F-G$, however it is shared with P3 during G. The filling ratio at the end of G can be found by considering that the charge has stayed under P2 only during G, because $t_{shift}^H \gg t_w^V$. The solution is given by (4.5), using $r_f^D(P2)$ for the initial occupation, t_{shift}^H for the time and 2 times lower charge density. The signal is transferred to P3 at the beginning of the next period B', during which the traps emit into the same signal packet. The ratio $r_f^{B'}(P2)$ can be written as

$$r_f^{B'}(P2) = r_f^G(P2)\ \exp\{-(t_w^V - t_w^{min})/\tau_e)\}, \tag{4.19}$$

and the CTI from the phase P2 is

$$CTI(P2) = \frac{N_t}{n_s}\{r_f^{B'}(P2) - r_f^D(P2)\}. \tag{4.20}$$

The calculation of the CTI, caused by the region under P3 is the most complicated. First, the trap occupation at the end of the interval F has to be found. This is done in two steps. The ratio $r_f^C(P3)$ is found from (4.5) for the dark current staying only under P3 during $B-C$ with initial occupation of $r_f^A(P3)$. Then the traps emit during the time $D-E-F$ and the filling ratio at the end of F is

$$r_f^F(P3) = r_f^C(P3)\ \exp\{-2\ (t_w^V - t_w^{min})/\tau_e\}. \tag{4.21}$$

At the beginning of G the charge arrives shared with P2 and stays during the horizontal shift, then the signal is only under P3 during the next interval $B'-C'$. The occupation

$r_f^{C'}(P3)$ can be found by applying (4.5) consecutively for the intervals G and $B' - C'$. The charge is finally emitted towards P1 during the next $D' - E'$ intervals and

$$r_f^{E'}(P3) = r_f^{C'}(P3)\,\exp\{-(t_w^V - t_w^{min})/\tau_e)\}. \tag{4.22}$$

The CTI from P3 can be written as

$$CTI(P3) = \frac{N_t}{n_s}\{r_f^{E'}(P3) - r_f^F(P3)\}. \tag{4.23}$$

The vertical CTI per pixel is given by

$$VCTI = CTI(P1) + CTI(P2) + CTI(P3). \tag{4.24}$$

The initial occupancies $r_f^A(P1)$ and $r_f^A(P2)$ can be found in the way described before.

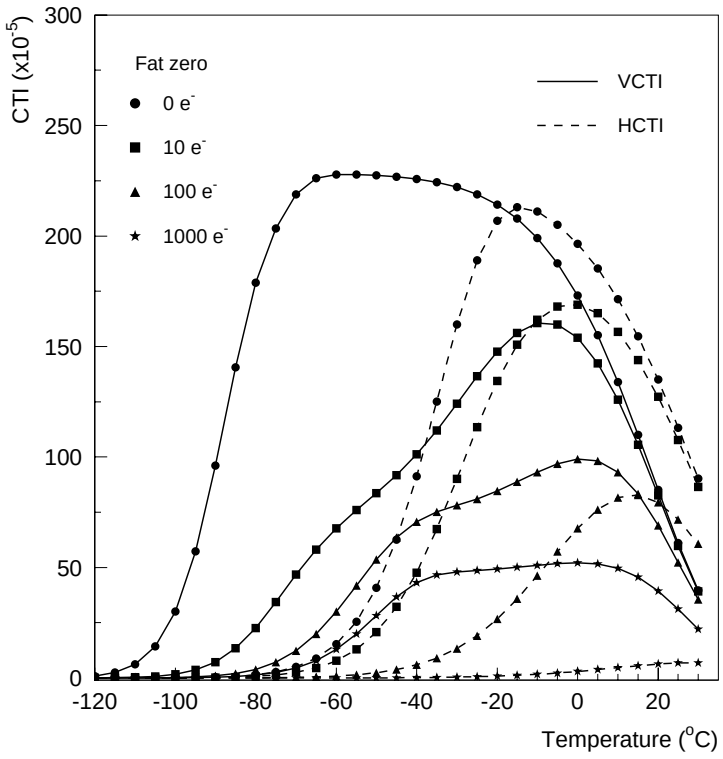

Figure 4.7: Modeled HCTI and VCTI as a function of the temperature and of the background charge in 3-phase CCD. The defect is taken to be the $V - V^-$ center with a concentration of $5{\times}10^{10}$ cm^{-3}. Widths of the clock pulses are $t_w^H = 2$ μs, $t_w^{min} = 0.67$ μs, $t_w^V = 4.67$ μs and $t_{shift}^H = 1.8$ ms.

The CTI model of MPP mode 3-phase CCD is more difficult to build compared to the model of 2-phase device. Particularly problematic is the modeling for the region under

the phase P1, because most of the time no charge is stored there and it is completely emptied during the horizontal shift. One would expect that the P1 can cause large CTI over a wide temperature range with little dependence on the background charges.

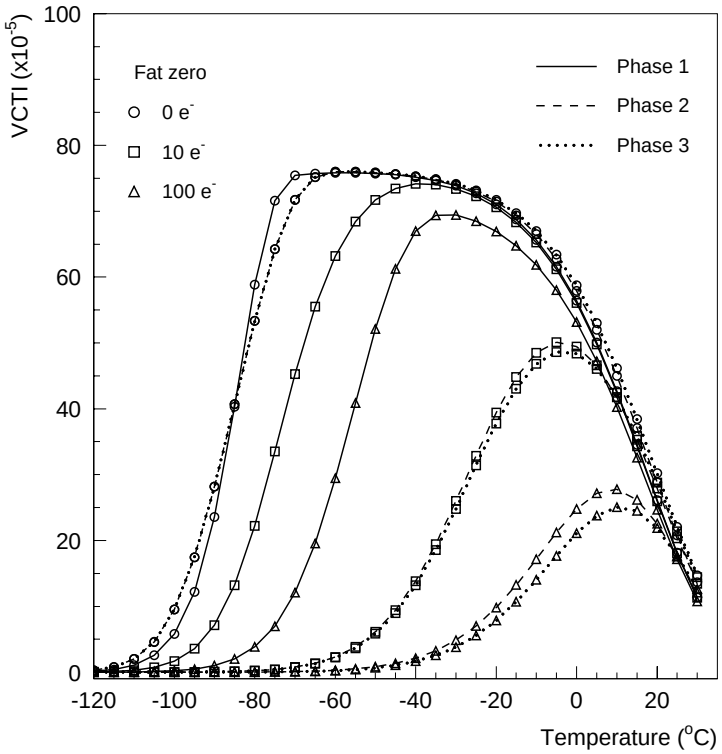

Figure 4.8: Modeled VCTI separately for the three phases as a function of the temperature and of the background charge. The conditions are the same as for the simulation on Fig. 4.7. At fat zero = 0 the VCTI curves of the phases P2 and P3 coincide.

The CTI as a function of the temperature and background charges in 3-phase CCD was simulated for the parameters of the EEV CCD02-06 and signal charge of 1620 electrons. The modeled CTI dependence on the background charge was studied for the same defect and defect concentration as for the 2-phase CCD. The well size is taken as $22 \times 7.3 \times 0.15$ μm^3 for 22μm square pixels. The modeled CTI on Fig. 4.7 is very similar to that presented on Fig. 4.3 for 2-phase device. The widths of the shift pulses correspond to the values used in the experiment at readout speed of 250 kpix/s. The strong decrease of the HCTI with the dark charge is observed as well as the weaker dependence for the VCTI. The HCTI peak is at higher temperature than the VCTI peak because $t_w^V > t_w^H$. It can be seen, that the CTI in the 3-phase device is notably larger than that in the 2-phase CCD

for almost the same simulation parameters. This will be explained later in Section 5.2.2.

The characteristic shape of the VCTI curve at low temperature is caused by the specifics of the charge transport in the vertical register and particularly the region under P1. Figure 4.8 shows the simulated VCTI separately for the three phases as a function of the fat zero. As mentioned above, the dominant CTI source is the phase P1, because it is practically always empty and traps the maximum number of electrons. The P1 has weak dependence on the concentration of dark charge, because any trapped dark electrons are emitted during the long horizontal shift time and the traps are always "hungry". Later in Section 5.3 this issue is revisited to show, that at large background charges the phase P1 cannot be considered completely empty as predicted by the model.

4.4 CTI Measurements and Modeling

4.4.1 Results on 2-phase CCDs

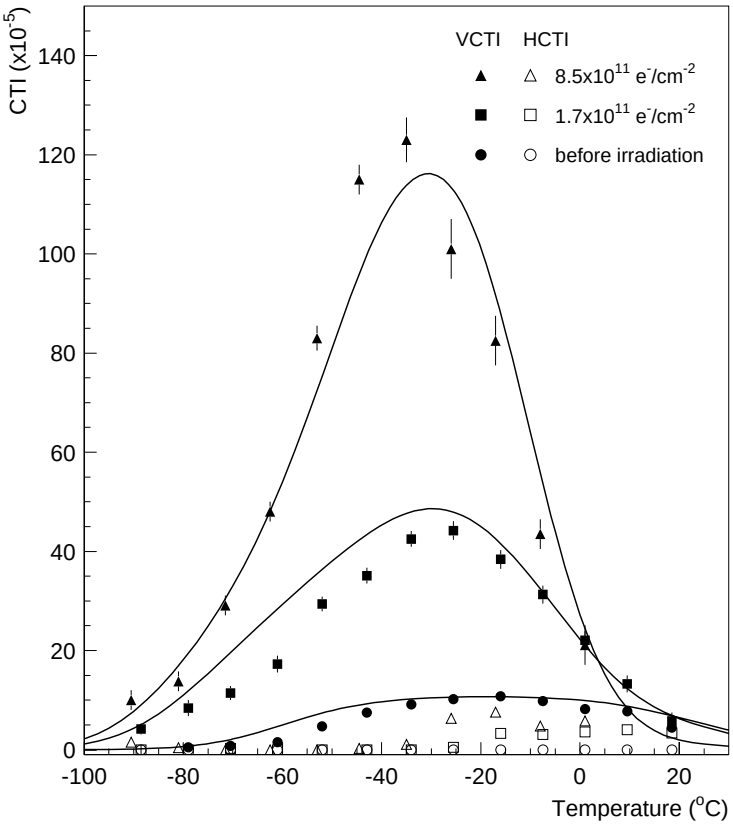

Figure 4.9: CTI as a function of the temperature and of the electron irradiation fluence in device #JS14/026. Symbols are the experimental data; solid lines represent the modeled VCTI for the combination of two traps at $E_c-0.37$ eV and $E_c-0.44$ eV. The concentration of the defect at $E_c-0.44$ eV is 9×10^9 cm^{-3}. The defect at $E_c-0.37$ eV has concentrations of 3.0×10^{10} cm^{-3} at 1.7×10^{11} e/cm^2, and 1.4×10^{11} cm^{-3} at 8.5×10^{11} e/cm^2.

The results from the CTI measurements on electron irradiated S5466 CCD, together with modeled results are shown on Fig. 4.9. Constant voltage swing of the vertical shift pulse ($V_{cc} - V_{ee}$) = 14V was kept throughout the measurements even if the value of V_{ee} had to be adjusted to operate the CCD in MPP mode. This was done in order to compensate for the flat band voltage shift. The other experimental conditions are described in Chapter 3.

Modeling was performed using the experimental values of the dark current on Fig. 3.9

and of the DCP on Fig. 3.10. It was found, that the DCP can be very well described by the expression

$$DCP\ (T) = A\ \exp\left\{-\frac{1}{\mathcal{E}}\left(b + T\frac{db}{dT}\right)\right\} + D_0\ \exp(-E_a/kT), \tag{4.25}$$

which matches the experimental data almost perfectly. The first term includes the contribution of the impact ionization, whereas the second one accounts for the thermal generation at high temperature. In (4.25) the parameter $E_a \approx 0.45$ eV is the activation energy of the thermally generated DCP and D_0 is its value at low temperature. An electric field of $\mathcal{E} = 10^5$ V/cm was used in the model.

It was found, that the pixels which do not contain X-ray generated charge cannot be considered empty during transfer. One of the reasons is, that the trail of deferred electrons spans over many pixels and the signal charge is transferred in a "pool" of very small background charge. Another reason is the presence of partially collected X-ray generated charge, which leads to the same effect. A few electrons can change significantly the pixel occupation and the CTI at low temperature, as shown on Fig. 4.3. Incorporation of small number of fat zero electrons proved to be necessary to explain the shape of the experimental CTI curves at low temperature. About 3 to 5 fat zero electrons gave very good match to the data and this correction was added to the model parameters.

The pre-irradiation VCTI is reasonably explained by the presence of a defect at E_c−0.44 eV with $\sigma_n = 3\times10^{-15}$ and a concentration of 9×10^9cm^{-3} (Fig. 4.9). Horizontal CTI before irradiation was below the measurable limit of 10^{-5}.

The modeling on electron irradiated CCDs showed that a trap at E_c−0.37 eV with $\sigma_n = 4\times10^{-15}$ cm^2 was responsible for the observed increase of the VCTI. The energy position of the trap, derived from the model, varies between E_c−0.37 eV and E_c−0.39 eV in three samples. The simulated results on Fig. 4.9 are based on the presence of two traps at E_c−0.37 eV and E_c−0.44 eV. The concentration of the trap at E_c−0.44 eV, obtained from the model increases insignificantly under irradiation. The introduction rate of the defect at E_c−0.37 eV is very close to a linear function of the electron fluence. The CTI of the horizontal register is less than 10^{-4} in the whole temperature range after irradiation. This result can be easily explained by the HCTI dependence on the background charge shown on Fig. 4.3. The peak in the HCTI, which would have occurred at high temperature is suppressed by the dark current pedestal and the exponentially increasing dark current.

Additional measurements with the extended pixel edge response technique (EPER,

[24]) were performed in order to verify the model and to confirm the creation of the defect at $E_c-0.37$ eV. The EPER technique is based on the emission of trapped charge with a time constant, defined by (4.1) into the overclock pixels, where there should be no signal in case of absence of bulk defects. By measuring the time constant of the deferred charge tail in the overclocked pixels of the CCD at different temperatures, it is possible to obtain the activation energy of the trapping defects. It was found, that sufficient trap filling, needed to observe the deferred charge was provided by the dark current. Using the above mentioned method, the energy position of the defect was estimated to be 0.40 ± 0.03 eV. This value is in a reasonable agreement with the energy obtained from the CTI model.

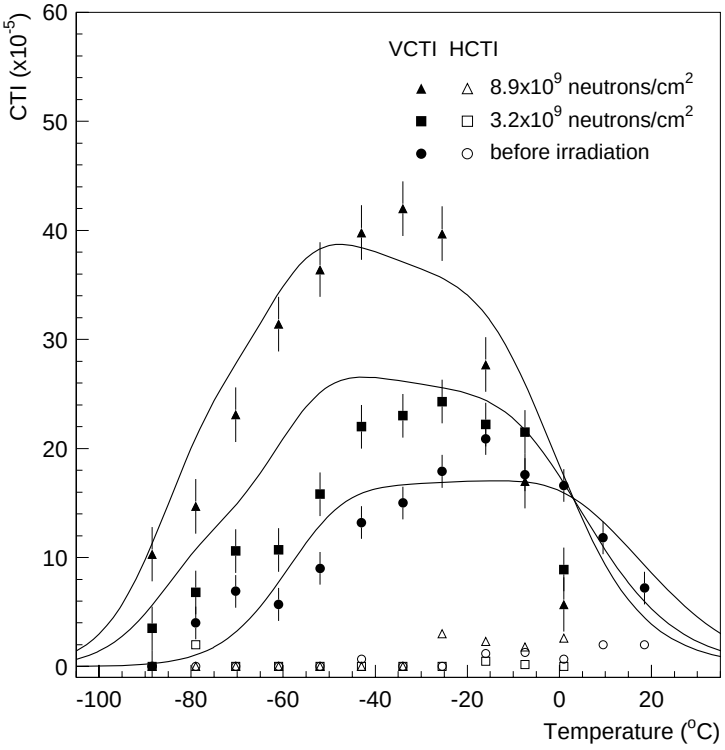

Figure 4.10: CTI as a function of the temperature in a neutron irradiated CCD (device #JS14/036). Symbols indicate experimental data; solid lines represent the modeled VCTI for the combination of two traps at $E_c-0.37$ eV and $E_c-0.44$ eV. The concentration of the defect at $E_c-0.44$ eV is 1.7×10^{10} cm^{-3}. The defect at $E_c-0.37$ eV has concentrations of 8.4×10^9 cm^{-3} at 3.2×10^9 n/cm^2, and 2.0×10^{10} cm^{-3} at 8.9×10^9 n/cm^2.

Having in mind the Poole-Frenkel effect, the observed defect in non-irradiated devices at $E_c-0.44$ eV is likely to be situated around $E_c-0.48$ eV. An exact identification of this defect is not possible using the available data. It has been either present in the silicon

wafers, or has been introduced during some of the manufacturing processes.

On Fig. 4.10 the experimentally obtained values of the VCTI in a neutron irradiated CCD are plotted together with the simulated results. The HCTI was below 5×10^{-5} in the whole temperature range before and after irradiation to 8.9×10^9 neutrons/cm^2. The VCTI data of a undamaged device is well described by the defect at $E_c - 0.44$ eV. After neutron irradiation, the fit of the model to the data showed that the same defect at $E_c - 0.37$ eV caused increase in the VCTI. The measured creation rate of that center is about 10 times larger than that observed in the electron irradiated devices. The HCTI was not modeled, because the experimental values are too small to enable comparison with the theory. The agreement with the experiment is deteriorated at high temperatures, probably because the charge of the hot pixels reduces the measurable VCTI by the fat zero effect.

4.4.2 Results on 3-phase CCDs

The experimentally determined CTI in an electron-irradiated 3-phase CCD02-06 is shown on Fig. 4.11. The model for the VCTI agrees very well with the data. However, the experimental HCTI values are about 2 times lower than the model predictions, the reason for which is not completely understood. The CTI, calculated for a defect at $E_c - 0.38$ eV is a very good match to the data. The similar characteristics of this defect and the trap, observed in the 2-phase devices imply, that they are probably the same. The calculated introduction rates of this defect in the Hamamatsu and EEV devices are within 22% of each other. The pre-irradiation values are VCTI $\approx 2 \times 10^{-4}$ and HCTI $\approx 10^{-4}$ [43]. The pre-irradiation CTI, not shown on the graph, is flat and without features.

As mentioned before, a small fat zero of 3 e$^-$ is incorporated in the model to account for the detrapped electrons and split X-ray events. This is needed to match the experimental data at low temperatures. The DCP was not observed in the EEV devices, which made the CTI modeling easier. The experimental values of the dark current were included in the simulation for the calculation of the initial filling ratios and the CTI.

The modeled HCTI for neutron-irradiated EEV device is very close to the experimental data, however the VCTI values do not match the results (Fig. 4.12). The experimental VCTI peak is somehow narrow, which is impossible to simulate for any parameters of the defects. The pre-irradiation VCTI is below 10^{-5}, therefore there is no interference with any other defects. The sharper decrease of the VCTI at $T > -40°C$ is probably due to

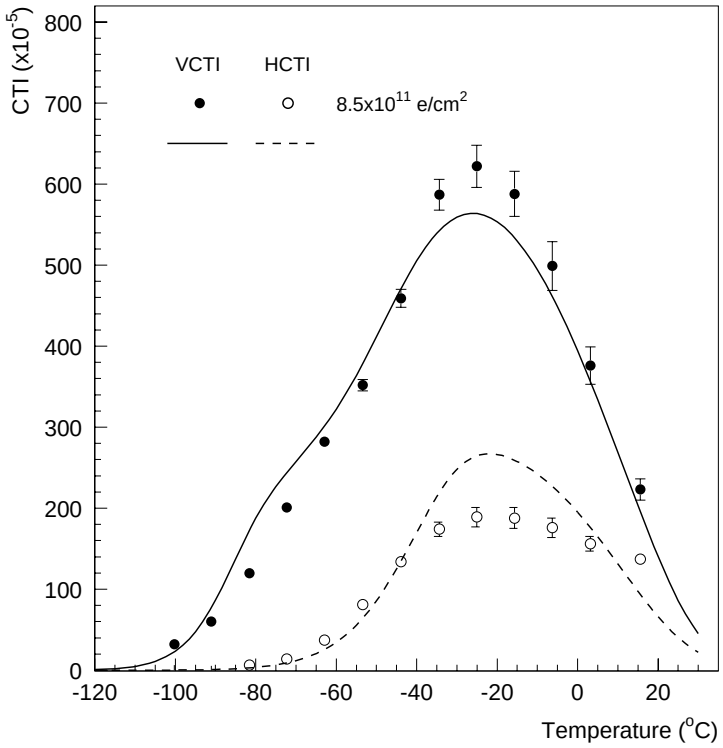

Figure 4.11: Temperature dependence of the CTI in electron-irradiated EEV CCD02-06 (#A4003-18). Symbols indicate experimental data; lines represent the modeled CTI for a defect at $E_c - 0.38$ eV with $\sigma_n = 4 \times 10^{15}$ cm^2 and concentration of 1.7×10^{11} cm^{-3}. The modeled HCTI values are multiplied by 1/2.

the influence of the hot pixels, because the dark current they generate becomes important in that temperature region. The peak in the pre-irradiation HCTI at about 0 °C is also difficult to explain.

From the simulation data it appears, that the creation rate of the defect at $E_c - 0.38$ eV is about 10 times larger than in the electron-irradiated device. The same was observed in the Hamamatsu devices.

4.4.3 Defect Identification and Annealing

It was shown, that only one defect can successfully explain the radiation-induced CTI in 2- and 3-phase devices. In the modeling it is difficult to separate the effects of the defect energy and its capture cross section, and the exact identification of the trap at $\approx E_c - 0.37$ eV is not straightforward. Taking into account the results on field-enhanced

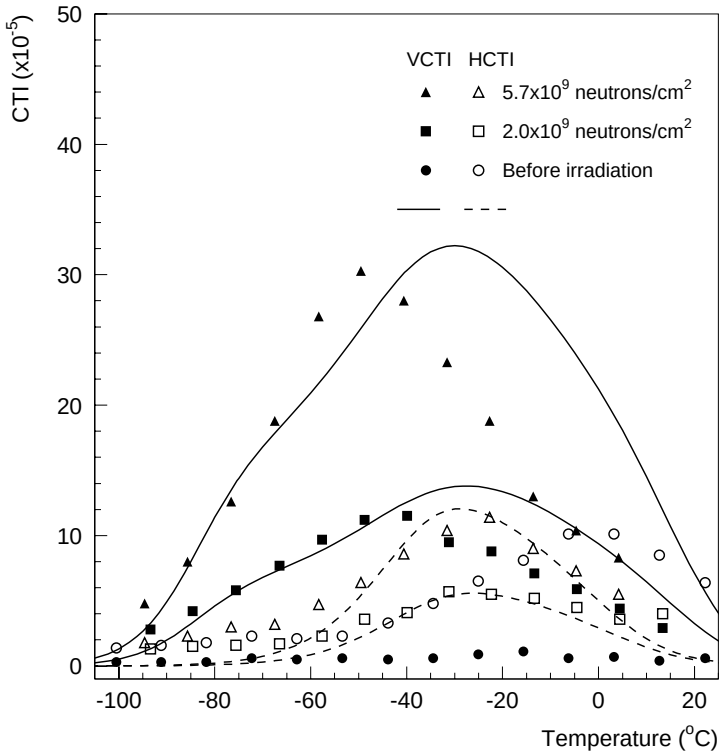

Figure 4.12: Temperature dependence of the CTI in neutron-irradiated EEV CCD02-06 (#A6041-48). Symbols indicate experimental data; lines represent the modeled CTI for a defect at $E_c - 0.38$ eV with $\sigma_n = 4 \times 10^{15}$ cm^2. The defect concentration at 2.0×10^9 neutrons/cm^2 is 5×10^9 cm^{-3}; for fluence of 5.7×10^9 neutrons/cm^2 the concentration is 1.2×10^{10}. The modeled HCTI values are multiplied by 1/2.

emission in hot pixels, presented in Section 3.2.4, we should consider the suggestion, that the observed defect at $\approx E_c - 0.37$ eV may be a center, which apparent energy position has been reduced by the Poole-Frenkel effect. We should assume that the variations of the barrier lowering near the potential minimum of the buried channel are not so large than those observed in the hot pixels, because charge transport takes place in a small volume.

Considering the potential lowering of 0.04 eV, calculated in Section 3.2.4, the defect at $E_c - 0.37$ eV might be the E or $V - V^-$ center, or the combined effect of both, because they are difficult to be resolved in our measurements. The results of Tokuda *et al.* [20] on silicon with similar phosphorus doping as of the buried channel of the S5466, strongly suggest that $V - V^-$ and $E-$ centers appear as a common peak due to their close energy levels. From annealing studies they conclude that about half of the defects in the observed trap level at $E_c - 0.39$ eV are $E-$ centers.

To verify the contribution of $E-$ centers to the observed VCTI peak, an annealing experiment was carried out on a Hamamatsu device irradiated to 4.3×10^{12} e^-/cm^2. The device was heated for 2 hours at 150°C, because it is known that the E center anneals at this temperature [20][21][25]. A decrease in the VCTI of about 60% was measured after the annealing, which is consistent with the suggestion that the observed defect at $E_c-0.37$ eV contains both $V-V^-$ and $E-$centers. The DCP also partially anneals, which contributes to the large uncertainty of this measurement. The $V-V^-$ and $E-$centers are usually observed in irradiated CCDs, with some results presented in Table 2.1. Because of the high phosphorus doping in the buried channel, the $E-$center is the dominant defect, as already discussed in Chapter 2.

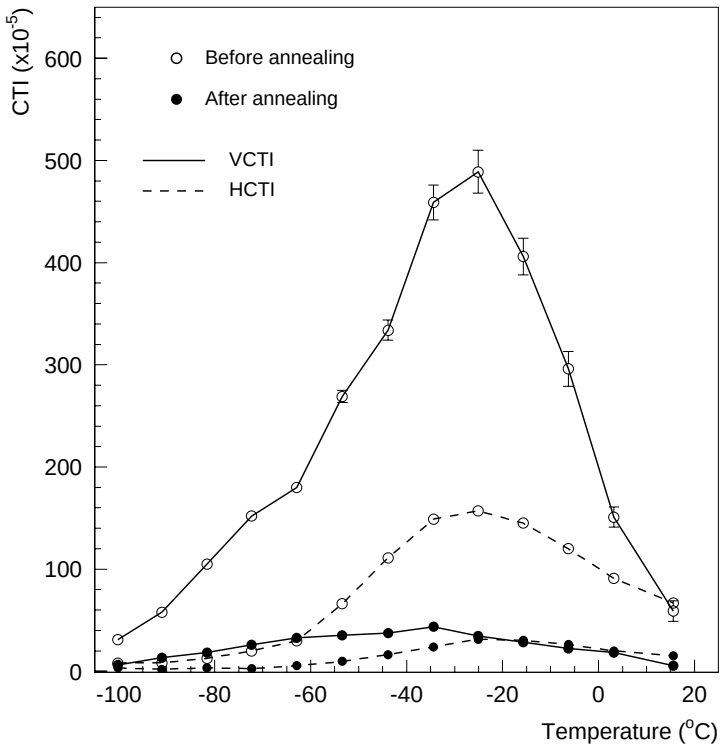

Figure 4.13: Temperature dependence of the CTI in electron-irradiated to 8.5×10^{11} cm^{-2} EEV CCD02-06 (#A4003-18) before and after annealing at 150°C for 2 hours.

The electron irradiated EEV CCD was annealed at 150°C for 2 hours as well. The absence of DCP in that device allows for better identification of the defects and their relative concentrations. Figure 4.13 shows the VCTI and HCTI of that CCD before and after the annealing. After the anneal the VCTI decreases dramatically to $\approx 4 \times 10^{-4}$,

which is about 2 times the pre-irradiation VCTI. Similar reduction can be observed for the HCTI. This result indicates, that the $E-$center is dominant in the EEV CCD, with almost no contribution from the divacancy.

Annealing can be used for restoration of the CTI of CCDs, working in radiation environment. It can be performed periodically, provided that the CCD support is designed to withstand the high temperature.

Chapter 5

Methods for CTI Improvement

In Chapter 2 it was pointed out, that the main radiation effects in CCDs are the flat band voltage shifts, interface and bulk dark current and the charge transfer inefficiency. It is widely considered, that the reduction of the radiation-induced flat band voltage shift is purely technological issue. There are reported CCDs in the literature, which can work after irradiation with doses approaching 1 Mrad. This is achieved by optimizing the manufacturing process to obtain "radiation hard" thin oxides. The interface dark current, which is much larger than the bulk one, is not regarded to be a significant problem because the MPP technique can successfully suppress it. The CTI is more complicated issue, because there is no universal solution to the problem, especially at high temperatures.

High CTI can be a serious limiting factor to the CCD application in radiation environment [43, 53]. At the future Linear Collider, for example, the accumulated 10-year mixed electron and neutron fluence is expected to reach $\sim 1.5 \times 10^{12}$ e^+e^- pairs/cm^2 and $\sim 5 \times 10^9$ neutrons/cm^2. Our estimations show, that the VCTI of EEV-type 3-phase CCD can reach values greater than 10^{-1} after such an irradiation. In the calculation we have supposed that the e^+e^- pairs are 10 times more damaging than the $\beta-$rays from a ^{90}Sr source.

On the other hand, the charge, generated by MIPs is about 1080 electrons in a 10μm-thick epitaxial layer. VCTI of the order of 10^{-2} means that the MIP signal will be lost after only a few transfers. To avoid that, measures have to be taken to reduce the CTI to acceptable levels. As was shown in (2.5), it is beneficial to have low transfer losses, because it allows one to have larger number of transfers, i.e. to build large area CCDs.

The considerations on the charge transfer in 2- and 3-phase CCDs, presented in Chapter 4 have given us the framework for understanding the mechanism of transfer losses.

The model and the simulation results, backed with experimental data have shown, that the CTI depends mainly on the following parameters:

1) **Concentration and type of the defects**. CTI is proportional to the defect concentration N_t (4.8), and defect parameters enter the emission and capture time constants τ_e (4.1) and τ_c (4.2);

2) **Temperature**. The dependence comes mainly from τ_e and it is very weak in τ_e, however the temperature affects the CTI in an indirect way through the background charge, provided by the dark current;

3) **Timing of the transfer**. The time available for emission and capture of electrons enters all the CTI formulae presented in Chapter 4;

4) **Density of the signal packet**. The CTI is reverse proportional to the signal density n_s (4.8);

5) **Background charge**. Its presence and concentration determines the trap filling ratio before the arrival of the signal packet, i.e. the number of defects capable of trapping signal electrons;

6) **Pixel occupancy**. It affects the CTI in a way analogous to the background charge. The trap filling ratio before the arrival of the signal is a function of the distance (in number of pixels m) between two consecutive charge packets, as shown in Chapter 4.

It should be noted, that only the first parameter can be considered as something that is fixed for a certain experiment. The other five parameters can be regarded as experimental conditions, therefore the CTI measurements are very sensitive to the way they are conducted. In this Chapter the results from the charge transfer model and the CTI measurements are applied and further extended in a search for methods to reduce the radiation-induced charge losses in CCDs.

5.1 Timing of the Charge Transfer

5.1.1 Readout Speed

As was shown in Chapter 4, the CTI is very sensitive to the length of the charge dwell and emission time periods. Shorter charge dwell time decreases the possibility of carrier capture and longer emission time results in more released electrons re-joining their packet. It is thus possible to improve the CTI by minimizing the dwell time and maximizing the emission time. For the serial register it is more reasonable to minimize the charge dwell

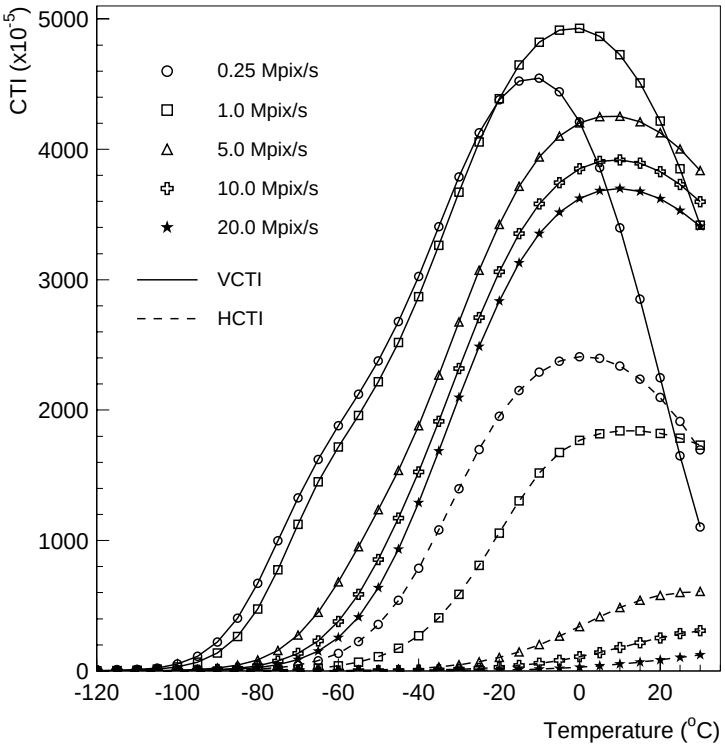

Figure 5.1: Simulated frequency dependence of the CTI in a 3–phase CCD for a defect at E_c-0.39 eV with concentration of 1.1×10^{12} cm^{-3}. This corresponds to ^{90}Sr–equivalent irradiation of $\approx 5 \times 10^{12}$ electrons/cm^2.

time, which corresponds to higher readout frequency, than to increase the emission time, which results in longer readout time.

The charge dwell time in the vertical register is equal to the horizontal shift time, which cannot be made very short ($\sim$ 100 ns) to reduce the trapping. Therefore the option here is to maximize the emission time, which will be discussed in the following section.

If the ratio of the pulse widths for the both registers is fixed, the effect can be sought only by varying the readout speed with the standard clocking pattern. Such a simulation was carried out to study the possible improvement of the CTI. Figure 5.1 shows a simulated dependence of the VCTI and HCTI for a 3-phase CCD. At speeds higher than several Mpix/s, horizontal CTI decreases rapidly because charge dwell time becomes shorter than the capture time constant τ_c of the defects. This shows an efficient way to fight the HCTI, and it is favored by the requirement to reduce the readout time by choosing higher clock frequency.

Vertical CTI is much less influenced by that, because the charge spends much longer time in the imaging section. The VCTI improves by only $\approx 30\%$ with the increase of the frequency from 250 kpix/s to 20 Mpix/s. This calculation shows that increasing the readout speed has only limited impact on the VCTI, and that other methods have to be employed to reduce it.

5.1.2 Clock Pattern

It is particularly interesting to apply the approach of variable dwell and emission times for CTI reduction to the vertical register, because it is where the dominant charge losses occur. As was pointed out in the previous section, the charge dwell time in the vertical register is always much larger than τ_c, therefore it is not possible to reduce the trapping. The solution should be sought in the increase of the emission time.

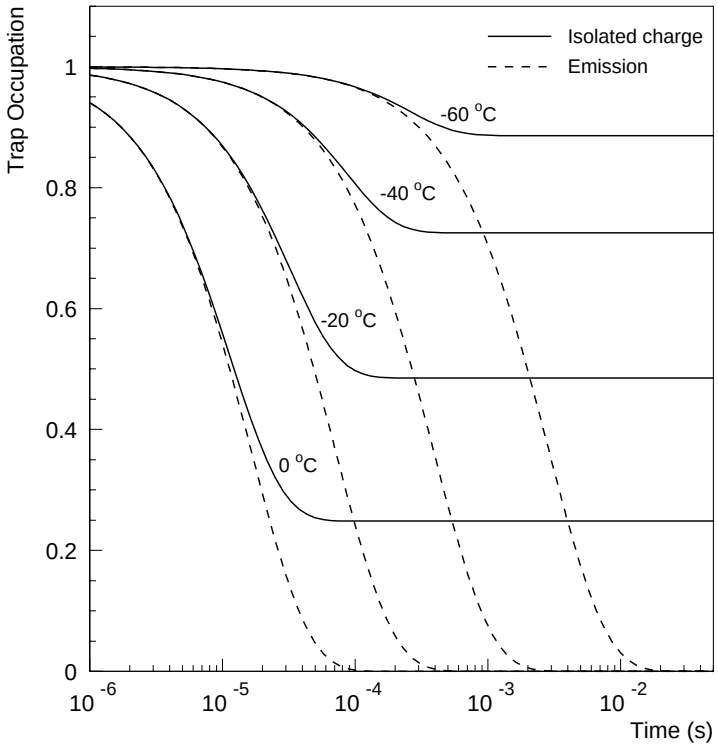

Figure 5.2: Simulated time evolution of the trap occupation in an isolated pixel at different temperatures (solid line) for a trap at E_c-0.39 eV. Dashed line is the calculated occupation in case of emission and release to neighboring pixels.

Let us consider the time dependence of the trap occupation in two cases. The first

one is when the electrons can freely leave the pixel, and the second case is when they are confined in the pixel volume. The dashed lines on Fig. 5.2 show the time evolution of the trap filling ratio r_f with time at different temperatures in the first case, starting from $r_f\ (t = 0) = 1$. It can be seen, that at low temperature the vertical shift pulse should be very long to allow large fraction of the trapped charge to be released. At high temperature this time becomes shorter in accordance with (4.1), and reasonably long vertical shift pulses can be used to reduce the CTI.

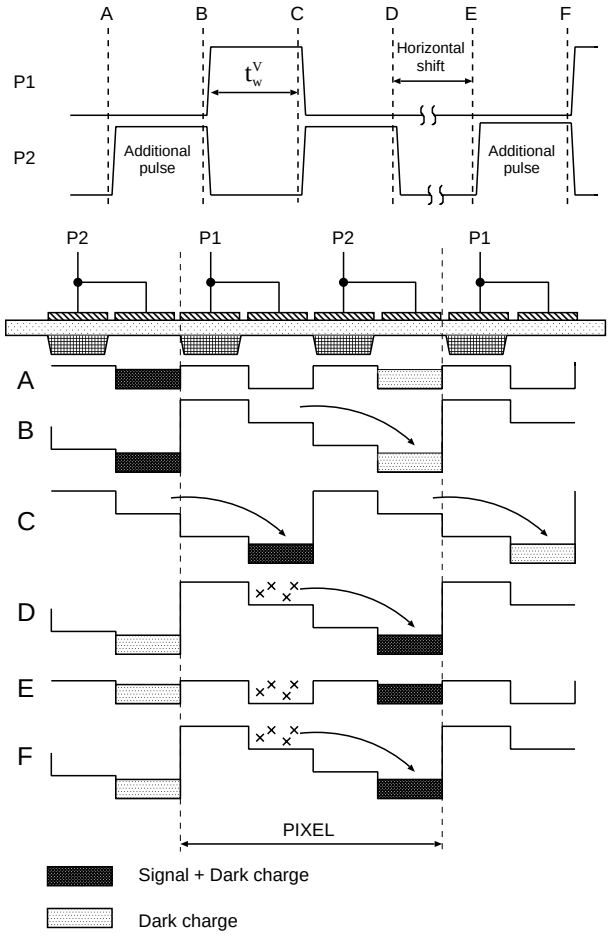

Figure 5.3: Modified vertical clocking pattern in 2-phase CCD, which can decrease the CTI.

Solid lines on Fig. 5.2 show the time evolution of the trap filling ratio in the same pixel in the second case, i.e., released electrons are not allowed to leave. After some time the defects emit electrons and the pixel reaches thermal equilibrium with trap occupation given from (4.4)

$$r_f^0 = \frac{\tau_e}{\tau_e + \tau_c}. \tag{5.1}$$

Such a condition is present under the phase P1 of a 2-phase CCD during the horizontal shift period ($C-D$), shown on Fig. 4.2. At the end of the period some part of the trapped charge is free, because sufficiently long time has passed to allow emission. On the other hand, the capture time constant is large enough not to re-capture the electrons because of the very small signal density (few electrons). However, these free electrons do not join their signal packet because they mix with the following charge during the period E. This can be avoided with the addition of another pulse to the P2 sequence (Fig. 5.3), so that to collect the released electrons back into their own signal packet.

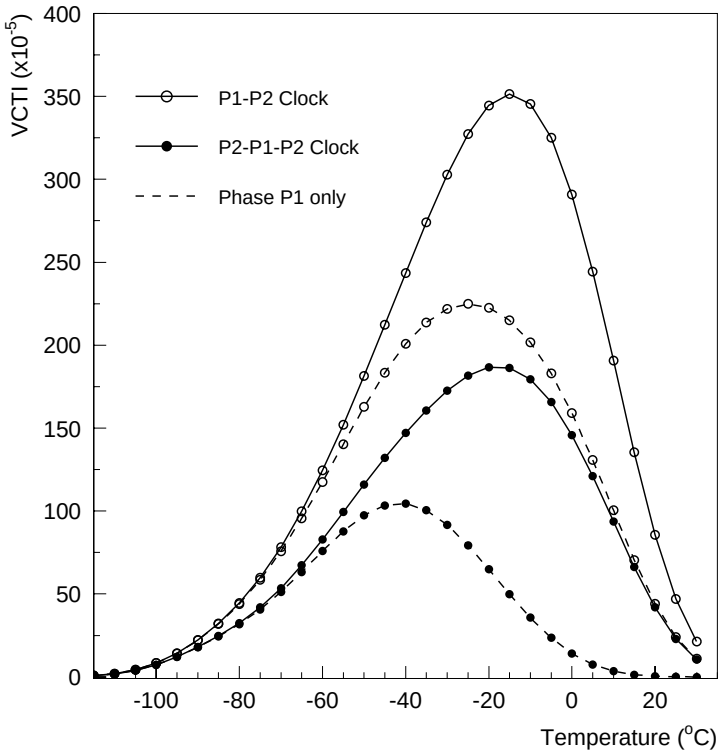

Figure 5.4: Simulated temperature dependence of the VCTI of 2-phase CCD, caused by defect at $E_c - 0.39$ eV with concentration of 2×10^{11} cm^{-3}. The width of the shift pulses t_w^V is 8μs and t_{shift}^H = 2.3ms at 250 kpix/s.

The horizontal shift time is relatively long ($\sim 100\mu$s), so that most of the trapped electrons will be released at the end of the period E, according to Fig. 5.2. The next vertical transfer sequence begins with P2 = *high* and this allows one to collect the released electrons back into their packet to the end of the period F. This method should improve the CTI from the phase P1 by a factor, given as the inverse ratio of trap occupation in

equilibrium (5.1), with the effect shown on Fig. 5.2.

Figure 5.4 shows the advantage of using the modified sequence on Fig. 5.3 (P2-P1-P2) over the standard scheme (P1-P2) on Fig. 4.2. The VCTI, caused by the phase P2 does not change, however the VCTI from the phase P1 is reduced significantly. The improvement in the total VCTI on Fig. 5.4, measured at the peak, is about 1.8 times. In reality this factor is expected to be smaller, because some of the released electrons can be captured by other defects or can recombine with holes.

An attempt was made to prove this idea experimentally on electron-irradiated S5466 CCD. Defects, created by electron irradiation provide sizeable CTI for the measurement, however the DCP in those devices influences the results and it is not possible to observe the clean dependence on Fig. 5.4. The experimentally determined VCTI as a function of the clock width and pattern is shown on Fig. 5.5.

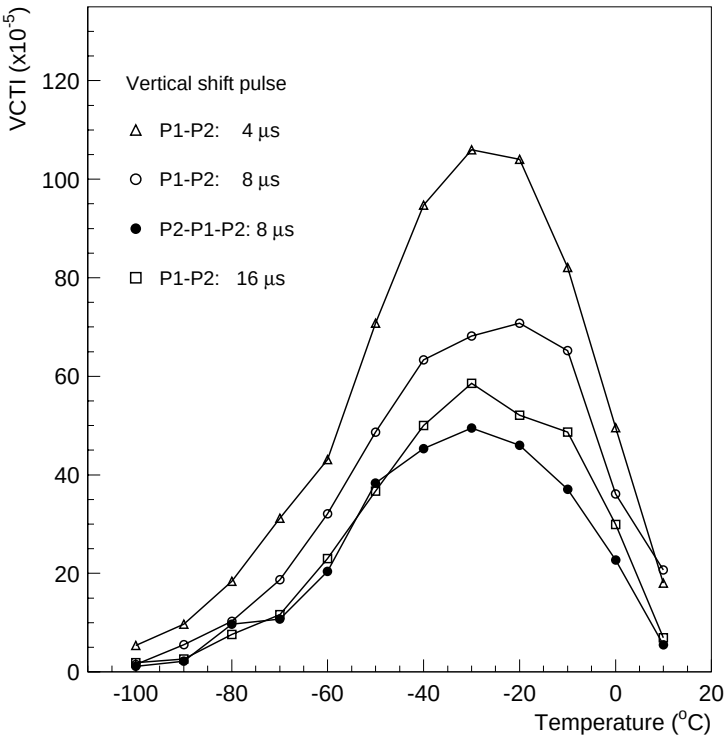

Figure 5.5: Temperature dependence of the VCTI of S5466 CCD (#JS8 053), irradiated to 8.5×10^{11} electrons/cm^2. The measurement was carried out using 3 different clock widths t_w^V and two clocking patterns for $t_w^V = 8\mu$s. The readout speed is 250 kpix/s.

As shown on Fig. 3.11, the DCP increases with the width of the shift pulse t_w^V. This

provides larger fat zero effect for longer pulses and results in lower measurable CTI. The P2-P1-P2 clocking has indeed lower VCTI than the standard sequence P1-P2 (Fig. 5.5), however the DCP with the P2-P1-P2 clocking is larger, because it is accumulated in 24μs ($3 \times 8\mu$s) instead of the 16μs ($2 \times 8\mu$s) for the P1-P2. Because of the influence of the DCP, it is difficult to draw a quantitative conclusion on the effect of the proposed clocking pattern.

However, one indirect evidence can be observed from the comparison of the CTI curves for 8μs P2-P1-P2 and 16μs P1-P2 pulses. The DCP for the 16μs P1-P2 clocking is accumulated in 32μs and it is larger that the DCP for the 8μs P2-P1-P2 sequence. Furthermore, the 16μs P1-P2 clocking has longer time available for emission of trapped electrons and its CTI should be still lower that that for the P2-P1-P2 pulses. However, the VCTI with P2-P1-P2 sequence on Fig. 5.5 is in fact lower than that for the standard 16μs P1-P2 clocking. This shows, that the proposed pulse pattern is more effective than simply increasing the widths of the standard shift pulses, which is one of the model's predictions.

5.2 Influence of the Signal Density

5.2.1 Notch CCD

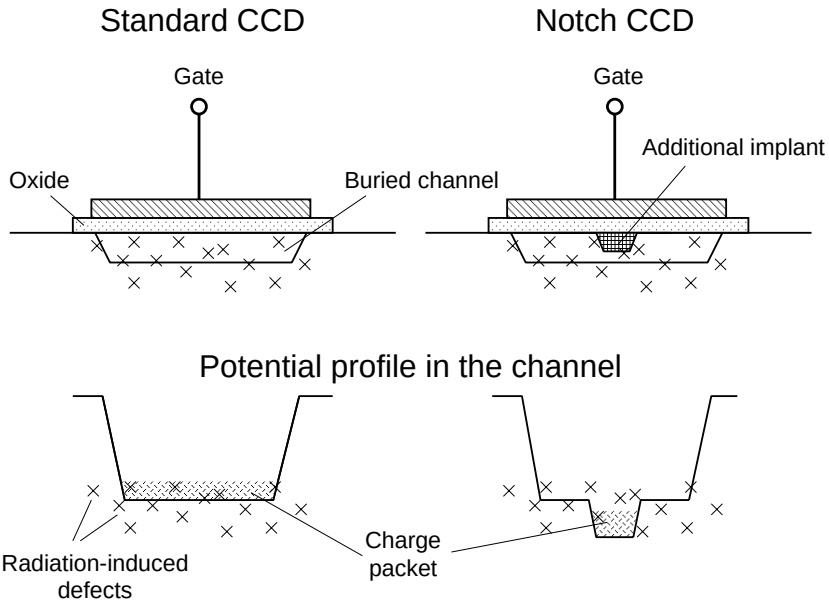

Figure 5.6: Schematic representation of a Notch CCD, showing that signal packets, confined in the notch encounter less traps on their way to the output.

One of the important methods for CTI improvement is to raise the charge density of the signal packet. It was shown, that the CTI depends on the concentration of signal electrons n_s as described in Chapter 4

$$CTI \propto N_t/n_s, \tag{5.2}$$

where N_t is the defect concentration. Because the signal usually varies very little (as in a vertex detector) and can be considered as being fixed, the signal density can be increased by forcing the same charge into a smaller volume.

One way to reduce the signal volume is to use an additional narrow implant in the CCD channel (Fig. 5.6). This implant forms a sub-channel, or "notch" in the potential profile of the transport channel, confining the signal charge into a fraction of the pixel volume and increasing the n_s. This concept was developed more than a decade ago for space applications [30]. It should be noted, that the CTI improvement is only for small signals (not bigger than $\sim 10^4$ e$^-$), because the notch full well capacity is reduced.

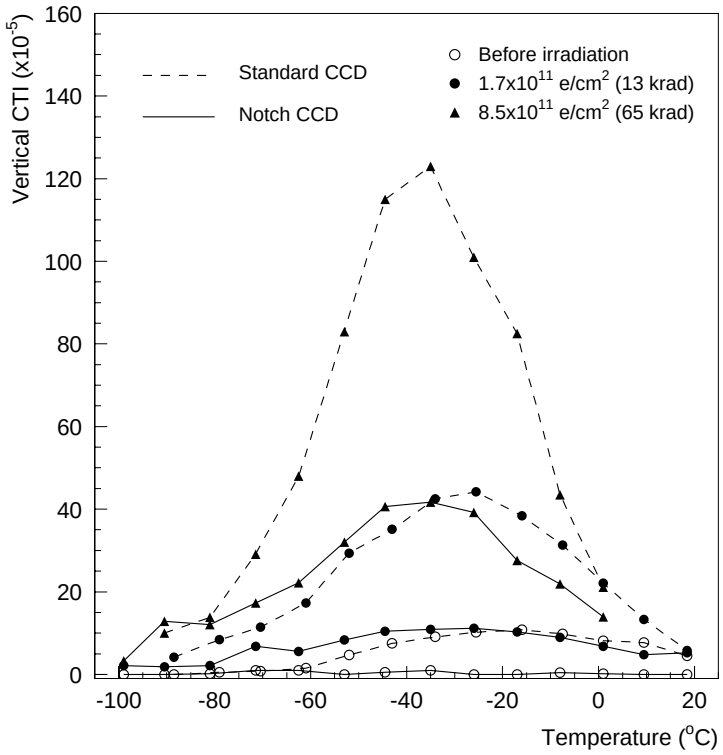

Figure 5.7: VCTI of notch (#P4 1-5B1P-2) and standard S5466 (#JS14 026) CCDs at 250 kpix/s. The DCP in the devices is almost the same.

The actual CTI improvement from the notch was measured on a electron-irradiated device, based on the Hamamatsu S5466 design. Due to the additional 3μm-wide notch channel, its VCTI is about 3 times lower than that in conventional S5466 device (Fig. 5.7). The VCTI and the HCTI in another notch CCD (#P4 1-5B1P-4) were measured to be $< 1 \times 10^{-4}$ at the highest reached neutron fluence of 5.7×10^{9} cm^{-2}, which is a very good result.

5.2.2 Differences Between 2- and 3-phase CCDs

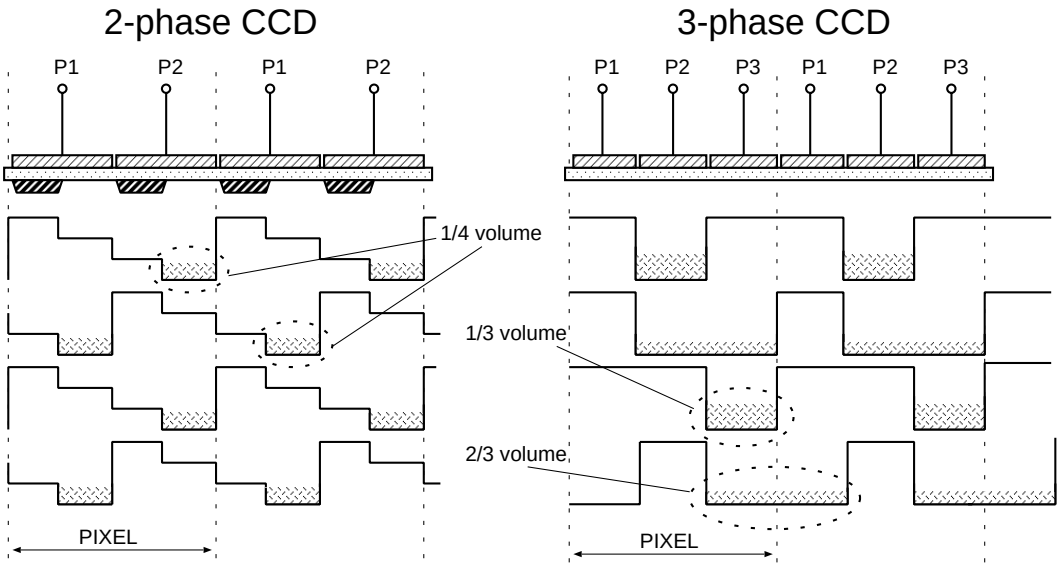

Figure 5.8: Charge transfer and storage volumes in 2- and 3-phase CCDs.

The 2- and 3-phase CCDs are the most widely used architectures today. Considering the charge transfer process, there are two important differences between them: the charge storage volume and the clock timing. In this section we will study how they can affect the CTI.

Using the CTI models for 2- and 3-phase CCD, developed in Chapter 4, this dependence was simulated for equivalent devices, with the only difference being the number of phases. The charge transfer and the corresponding volumes for storage in both devices are shown on Fig. 5.8. In 2-phase CCD the charge occupies 1/4 of the pixel volume, whereas in 3-phase CCD it fills 1/3 or 2/3 of it. It is therefore expected that the 2-phase CCDs should have lower CTI.

Indeed, the simulation revealed, that under equal conditions the 2-phase CCD had

about 2.5 times smaller CTI than the 3-phase device. This result comes mainly from the higher signal density in 2-phase devices and formula (5.2).

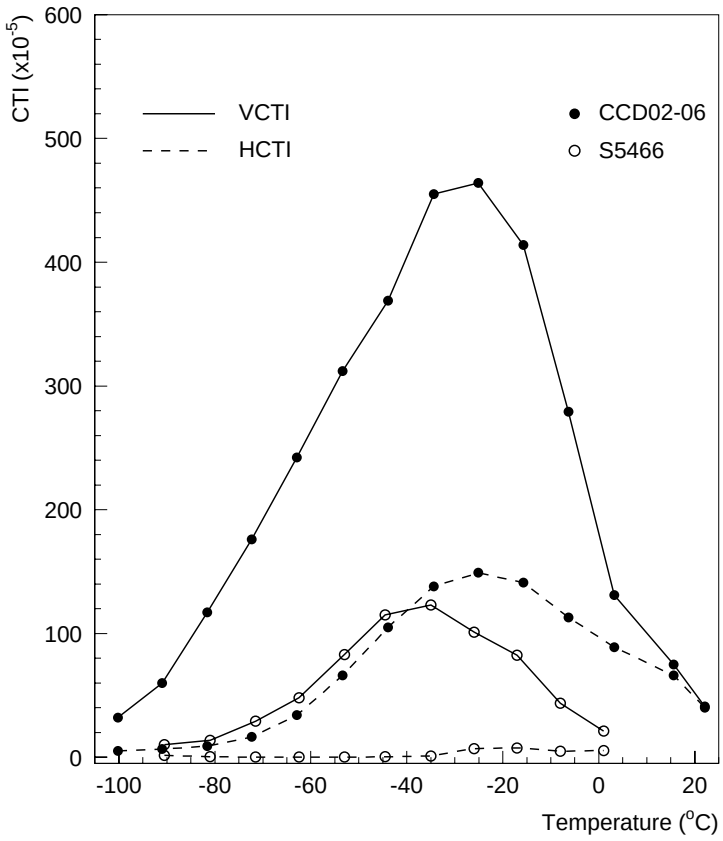

Figure 5.9: CTI of 2-phase (S5466) and 3-phase (CCD02-06) CCDs, irradiated with 8.5×10^{11} electrons/cm^2. The readout speed is 250 kpix/s.

A CTI measurement was performed on electron-irradiated 2- and 3-phase CCDs. It showed that the 2-phase CCD had about 4 times better CTI than the 3-phase one (Fig. 5.9). The experimentally observed difference is larger than predicted mainly because of the spurious dark charge in S5466 devices, which decreases the measurable CTI values by the fat zero effect. Under equal conditions, the difference in the CTI of 2- and 3-phase devices is expected to be close to the theoretically calculated value above. Because of this advantage, 2-phase devices should be preferred for applications where minimizing the charge transfer losses is important.

5.2.3 Pixel Size

Under the assumption, that the charge is stored in a constant volume, independent of the signal size for small number of electrons, one conclusion can be drawn for the dependence of the charge losses on the pixel size.

Let us consider, that the charge is stored in a volume $V_{eff} = \alpha a^2 d$, where a is the pixel size, d is the effective depth of the potential well and α is a coefficient. The CTI can be written in the form analogous to (4.8):

$$CTI = \frac{N_t}{n_s}\ \mathbf{F}(\tau_e, \tau_c, t_w), \tag{5.3}$$

where $\mathbf{F}$ is a function of the emission and capture time constants and of the width of the shift pulses. The charge density can be expressed as

$$n_s = \frac{Q_0}{V_{eff}} = \frac{Q_0}{\alpha a^2 d}, \tag{5.4}$$

where Q_0 is the number of signal electrons. By substituting (5.4) into (2.5), we get

$$Q_n = Q_0 \left(1 - \frac{N_t}{Q_0}\alpha a^2 d\ \mathbf{F}(\tau_e, \tau_c, t_w)\right)^n \approx Q_0 \left(1 - n\frac{N_t}{Q_0}\alpha a^2 d\ \mathbf{F}(\tau_e, \tau_c, t_w)\right). \tag{5.5}$$

If the number of transfers $n = L/a$, where L is the physical length of the CCD register, is substituted in (5.5), we obtain

$$Q_n \approx Q_0 \left(1 - L\frac{N_t}{Q_0}\alpha a d\ \mathbf{F}(\tau_e, \tau_c, t_w)\right). \tag{5.6}$$

Formula (5.6) shows, that the term responsible for the charge transfer losses is proportional to the product aL. This means, that in identical CCDs with the same L and different a, the CCD with the smaller pixels will have lower charge transfer losses. This conclusion can be confirmed by measurements on CCDs of the same type, in which only the pixel size is different. Such results on CCDs with pixel size of 48 μm, 24 μm (same chip size) and 12 μm (two times smaller chip size) have been published [56]. The data shows broadening of the ^{55}Fe spectra, caused by transfer noise from carrier capture and emission, which increases with the pixel size. Wherever possible, the CCD with the smallest pixel size should be used for improved CTI.

5.3 Injection of Background Charge

One of the most powerful methods, that can be used for CTI improvement is injecting of a sacrificial charge, or fat zero into the CCD registers. This charge reduces the CTI in

two ways: by increasing the signal charge density (5.2), as it is transported together with the signal; and most importantly, by filling the traps in front of the signal charge, so that less electrons can be captured. Figure 4.3 shows how even very small fat zero charge can dramatically decrease the CTI. The effect is very strong at low temperatures because of the longer emission time constant τ_e (Table 4.1). Once a defect captures an electron, it is occupied for a long time, during which the trap does not take part in the capture process.

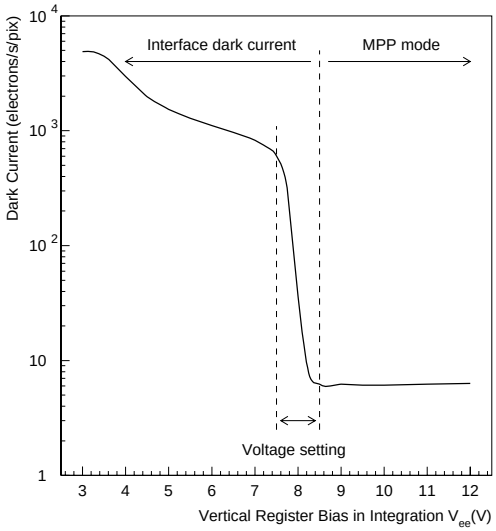

Figure 5.10: The principle of thermal fat zero generation.

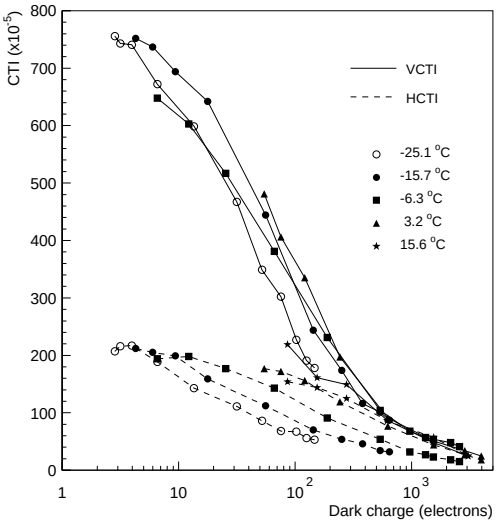

Figure 5.11: CTI reduction by fat zero effect in EEV CCD02-06 (#A4003-18), irradiated to 8.5×10^{11} electrons/cm^2.

The results in Chapter 4 have shown that the CTI of the vertical register dominates the charge losses in the CCD. However, introducing fat zero in the vertical register through the CCD injection port is not a trivial task because of the large non-uniformity of the injected charge [57].

Another way to add sacrificial charge is to use the device dark current. It is integrated in all the pixels through thermal generation, and can be controlled by choosing appropriate temperature and/or integration time. However, the number of dark current electrons increases as the signal moves closer to the output, which is just the opposite one would like to have.

For very short integration times the thermally generated bulk dark current in MPP mode CCDs may not be sufficient to cause significant CTI reduction. To overcome that,

another method to inject fat zero was developed, which employs the characteristics of the interface dark current. By varying the negative gate bias voltage of the vertical register V_{ee}, the CCD can be driven into semi-MPP mode and its dark current can be controlled between the MPP mode value and ≈100 times that value (Fig. 5.10). At high temperatures, this current can be sufficient to provide charge of the order of 1000 electrons even if the CCD readout cycle is very short. The proposed method works on any type of MPP CCD, because the fat zero is generated thermally. The amount of injected charge can be controlled either by adjusting the V_{ee}, or by setting V_{ee} to some low value and adjusting the amount of time, during which the CCD is out of MPP mode. Practical implementation of the proposed method depends on the irradiation level and requires precise adjustment.

One important feature of the proposed method is that it has the ability to self-adjust for non-uniformities of the surface damage defects. If in some pixels the flat band voltage shift is higher, corresponding to higher surface and bulk damage, larger dark current is generated automatically because the MPP threshold is larger (Fig. 5.10). This dark charge compensates for the higher CTI in those pixels.

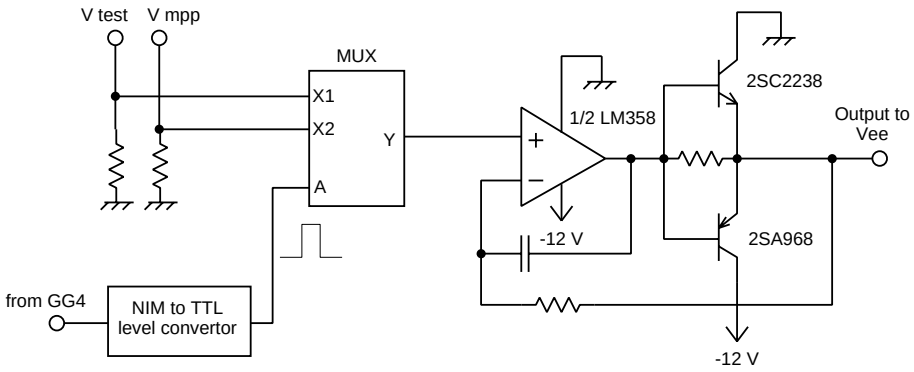

Figure 5.12: Simplified schematic of the circuit for variable V_{ee}^{V}. The input NIM signal is taken from the output of GG4 on Fig. 3.3.

The reduction of the CTI in electron-irradiated CCD was measured using the proposed method for thermal fat zero generation. The EEV CCD02-06 was chosen because of the absence of DCP, which would have made the result more difficult to interpret. The experimental data on Fig. 5.11 is obtained by adjusting the dark current via the V_{ee} voltage, using the circuit on Fig. 5.12. The result shows, that the CTI can be reduced several times by injecting fat zero of ~ 1000 electrons, which is comparable to the number of signal electrons (1620 e^-). The additional charge increases the noise by 32 e^- RMS,

however this would not degrade the performance of high-speed CCDs, which have noise of the order of 100 e^- RMS.

Estimations of the radiation-induced dark current after receiving combined electron and neutron fluence at the expected 10-year levels at the future LC show, that dark current injection of > 1000 electrons by this method can be achieved at temperatures $> 5°C$ and integration time of 6.7 ms. The requirement for the readout timing follows from the crossing rate of the bunch trains, which is 150 Hz. The CCDs have to be read out completely between the crossings.

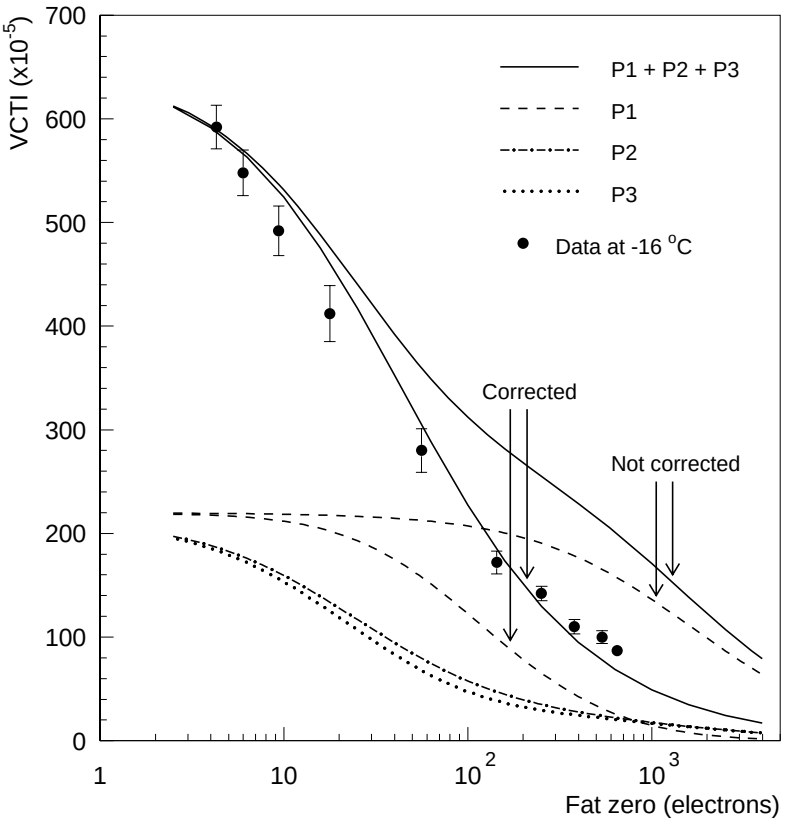

Figure 5.13: Simulated VCTI dependence on the background charge in EEV CCD02-06 (#A4003-18) for a defect at $E_c-0.38$ eV with the same parameters as those used in Fig. 4.11. Solid line is the total VCTI; dashed lines are the VCTI separately for the three phases; dots are experimental data at 8.5×10^{11} electrons/cm^2. Corrected VCTI of the phase P1 uses equation (5.7).

The CTI dependence on the fat zero charge in the EEV CCD was modeled using the

experimental CTI data. On Fig. 5.13 the simulated VCTI is plotted as the total value and separately for the three phases. The phase P1 is the cause of much of the VCTI at high dark charge, because it is essentially empty most of the time. Its VCTI decreases only because of the $1/x$ dependence on the charge density, which is a sum of the signal (1620 e^-) and the background charges. However, this dependence contradicts the experimental data, which implies that the phase P1 becomes partially occupied at high levels of the background charge. The model, presented in Chapter 4 does not contain elements capable of explaining this feature. The discrepancy may arise from the simplification of constant charge volume, which is embedded in the model, or from other reasons.

One simple correction to the model is to suppose, that the pixel occupation from the dark current under the phase P1 approaches that of the phases P2 and P3 for charges greater than ~ 100 e^-. Since from (4.15) $r_f^A(P1) \to 0$ for small charges, $r_f^A(P1)$ can be approximated with

$$r_f^A(P1) = r_f^A(P2) \left(1 - \frac{1}{1 + \frac{N_{fz}}{100}}\right), \tag{5.7}$$

where N_{fz} is the number of fat zero electrons. The corrected values of the VCTI of the phase P1 on Fig. 5.13 were calculated using the equation (5.7). They track the experimental data much better than the non-corrected simulation.

The independent CTI measurements at variable temperature and at variable dark current charge (but with fixed temperature) are helpful and allows one to better check the consistency of the charge transfer model.

5.4 Pixel Occupancy

Pixel occupancy affects the measured CTI by increasing the ratio of filled traps. It is particularly effective at low temperatures because of the long emission time constant. The CTI gets smaller as the pixel occupancy increases, because larger fraction of the defects are occupied and unable to trap signal electrons (Fig.2.3). Higher background increases the defect concentration and therefore the CTI in CCD, working in radiation environment. On the other hand, the number of hit pixels also increases, which leads to smaller CTI.

The dependence of the CTI on the density of hit pixels can be observed in measurements with an X-ray source. Pixel occupancy can be varied by selecting different time for X-ray illumination while keeping the same readout time and speed. The total number

of isolated pixel events should be the same to exclude errors from different statistics. To avoid any interference from the dark current, the measurement has to be carried out at low temperature.

Figure 5.14 shows such a measurement on a 3-phase EEV CCD. The CCD readout cycle was varied between 0.3 s and 5 s with fixed readout time of 0.18 s. Only the first 100 pixels of the CCD were read out to achieve sufficiently short readout time at 250 kpix/s. The density of the X-ray IPE changes as the shutter is open during integration and closed during readout. The CTI model showed, that the pixel occupation, caused by higher density of IPE is only one of the factors, leading to the observed decrease of the CTI on Fig.5.14. The density of split and partially collected charge also has influence on the CTI.

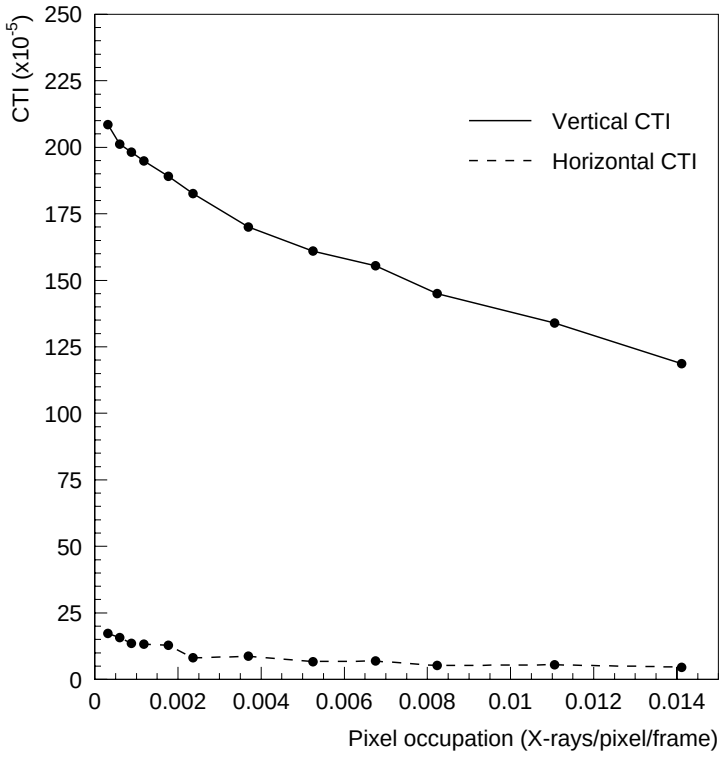

Figure 5.14: CTI dependence on the pixel occupancy at $-75°$C in EEV CCD02-06 (#A4003-18), irradiated to 8.5×10^{11} electrons/cm^2.

The typical pixel occupation, used in most of the CTI measurements in this and the previous chapter is about 0.002 IPE/pixel/frame.

5.5 Implications to the CCD Design

In this section the methods for CTI improvement, described above are applied to the design of a CCD, that can be used in the vertex detector at the future Linear Collider. As already mentioned, the expected radiation environment is challenging to the current CCD technology, and in particular concerning operation at near-room temperature. The CCDs usually have to be cooled to below $-70°$C to suppress the charge transfer losses [8]. Operation at normal temperature is attractive from the point of view of the designer of the vertex detector, because it allows the supporting CCD structure to be simplified. Additionally, the mechanical stresses and deformations, caused by the cooling can be avoided and the precision of the vertex detector can be improved.

If we consider, that the flat band voltage shifts at the expected radiation environment are acceptable, the main point of concern for near-room temperature application becomes the CTI. As shown in the previous chapter, the vertical register has dominant contribution to the charge transfer losses, because the HCTI is usually much smaller than the VCTI. Only the CTI caused by electron irradiation can be considered, because the expected neutron background of $\sim 5 \times 10^9$ cm^{-2} causes much smaller effect, as shown in the previous chapter. Let us apply some of the options for CTI improvement, described in this chapter, to an EEV-like 3-phase CCD. From the experimental data it was calculated, that the radiation-induced VCTI in such a CCD increases at a rate of

$$\frac{\Delta VCTI}{\Delta \Phi} \approx 1 \times 10^{-14} \text{ cm}^2, \tag{5.8}$$

where Φ is the irradiation fluence. This value holds for the clocking pattern used in the experiment, readout speed of 250 kpix/s and does not include the influence of the dark current. The electron irradiation has been assumed to have spectrum, identical to that of a ^{90}Sr source.

We will consider, that the VCTI peaks in the temperature region between $-10°$C and $20°$C, which represents the worst case. The electron irradiation is taken as 1.5×10^{12} cm^{-2} ^{90}Sr-equivalent per year, assuming that the e^+e^- pairs are 10 times more damaging than the $\beta-$rays from the source. In one operational year there are 10^7 seconds, or ≈ 116 days. Using only some of the options for CTI improvement considered in this section, the VCTI can be reduced more than 60 times, as described in Table 5.1. We will consider, that the HCTI has been reduced to 10% of the VCTI. The simulation studies and the

experimental results show, that this value may be even overestimated.

Table 5.1: Vertical CTI improvements.

Option	**VCTI improvement**
Raise the output speed to > 5 Mpix/s	≈ 1.3 times
Use 2-phase CCD	≈ 2.5 times
Use notch CCD	3 to 4 times
Inject fat zero ≈ 1000 e^-	6 to 8 times
Total improvement	≈ 60 to 100 times

From the large difference between the VCTI and the HCTI it follows, that one can build a CCD with large number of pixels in the serial register and much smaller pixel number in the imaging section. This corresponds to proportional dimensions of the CCD chip in the two directions.

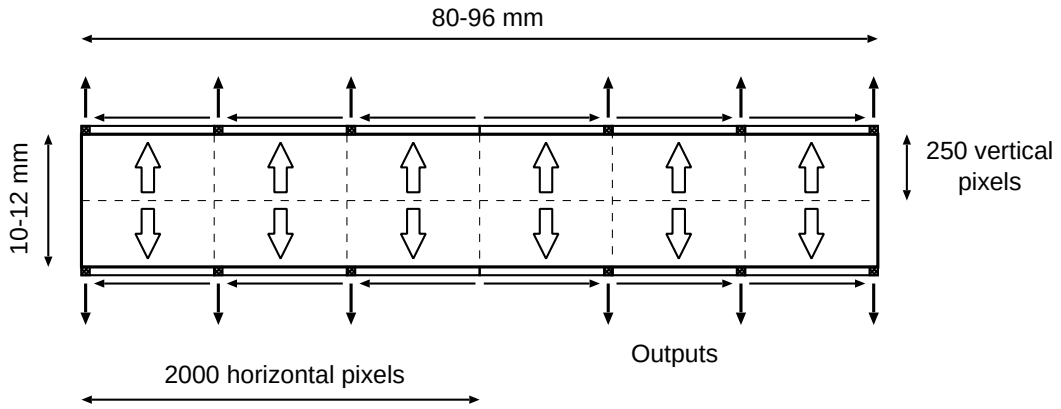

Figure 5.15: Model CCD with split readout, containing 2 Mpixels and 12 outputs. The smaller dimensions correspond to pixel size of 20 μm, the bigger ones to pixel size of 24 μm. Readout speed of 25 Mpix/s is needed to read all the pixels in 6.7 ms.

Let us calculate the operational time of the model CCD on Fig. 5.15, which has similar number of pixels and dimensions as the CCDs used in the VXD3 vertex detector. Devices with such parameters are likely to be used at the future Linear Collider. Split readout is implemented because of the requirement for complete readout in 6.7 ms. First, we have to consider the maximum acceptable charge losses in the device. If the limit to total losses is set to $<$ 25%, then from (2.5) we have the condition

$$(1 - VCTI)^v \ (1 - HCTI)^h > 0.75, \tag{5.9}$$

where $v = 250$ and $h = 667$ are the number of pixels in the vertical and in the horizontal register, correspondingly. It is easily calculated, that the condition (5.9) is fulfilled for the CCD on Fig. 5.15 if its VCTI $= 9 \times 10^{-4}$ and HCTI $= 9 \times 10^{-5}$. Despite the smaller number of pixels, the losses in the vertical register are about 20%, whereas only 6% of the charge is lost in the serial register.

This 60-times improved CTI corresponds to electron fluence of about 5.4×10^{12} cm^{-2}, or about 3.6 years of operation. Without all the measures, presented in Table 5.1 the CTI would reach the maximum allowed charge losses at a fluence of 9×10^{9} cm^{-2}, which corresponds to lifetime of only 22 days.

The uncertainties to this estimation come from the unknown energy spectrum of the irradiation at the future Linear Collider, which does not allow to calculate precisely the radiation-induced CTI. Better determination of the lifetime of the CCDs depends on how good the information about the e^+e^- background is. Another uncertainty comes from the poor knowledge on the scaling of the CTI with the energy of the irradiating electrons and positrons. In this calculation it was assumed, that they are 10 times more damaging than the ^{90}Sr electrons.

Such high speed CCD should not be difficult to manufacture, because the theoretical maximum clocking frequency for pixel size of 20 μm is about 62 MHz [58]. There is significant experience with multi-output large area CCDs for astronomy and high energy physics applications, and the future for much more challenging device architectures looks promising.

Summary

A systematic and detailed study of the radiation damage effects in 2- and 3-phase Charge Coupled Devices (CCD) has been conducted. CCDs are one of the primary options for tracking devices at the future vertex detector of a future Linear Collider due to their high precision and two-dimensional resolution. The backgrounds near the interaction point impose considerable challenges to the tolerance of the CCD sensors to radiation damage effects. To estimate the effects from the expected radiation background, surface and bulk damage have been extensively studied in electron- and neutron-irradiated CCDs from two different manufacturers, Hamamatsu Photonics and Marconi Applied Technologies.

Special attention was paid to the application of CCD in radiation environment at near-room temperatures. Multi Pinned Phase (MPP) mode CCD, which offer more than an order of magnitude lower dark current than conventional devices were studied. The flat band voltage shifts, caused by ionizing radiation have been found to be considerable, especially in devices irradiated under bias. In Hamamatsu devices additional dark signal, induced by the clocking was observed and found to be a major device problem. That current is explained by impact ionization from holes, emitted from radiation-induced defects at the Si-SiO_2 interface.

Dark current spikes ("hot pixels"), some of which generate current in the form of Random Telegraph Signals (RTS) were found in neutron irradiated devices. It was shown, that although potentially dangerous, RTS are unlikely to be a limiting factor to the device application at sufficiently fast readout even at room temperatures.

Charge transfer losses, or Charge Transfer Inefficiency (CTI) in CCDs, caused by radiation-induced bulk defects was one of the major issues under study. Charge losses in 2- and 3-phase CCDs, which are nowadays the most widely used devices, were studied both theoretically and experimentally. A model for the charge transfer in CCDs was built, which is one of the most important results presented in this thesis. The model allows one to study the influence of the clock timing and pattern, temperature, dark current and

other CCD parameters on the CTI. The experimental results on electron- and neutron-irradiated CCDs are in a very good agreement with the model predictions. The clock frequency and the dark current are shown to have larger influence on the CTI of the serial register than on the vertical register because of the different clocking schemes in the two sections.

The importance of the clock pattern for reducing the charge losses in the imaging section in 2-phase CCDs was shown. A modified clock pattern, which can decrease the vertical CTI by ≈ 1.8 times was developed and tested. It was shown, that the most effective method for minimizing charge losses is filling the traps by an additionally injected charge ("fat zero") in the device. A new method for thermal generation of fat zero effect in MPP CCDs is proposed, which offers several advantages and can be applied at near-room temperature on a variety of devices.

The results on radiation-induced CTI contribute significantly to the better understanding of the problem and offer solutions for minimizing the effects of bulk traps on the performance of CCDs. The results of this study can be used for building better, radiation-resistant CCDs and to optimize their operating conditions for reducing the influence of radiation defects on the device characteristics.

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