PROCEEDINGS OF SCIENCE

Progress in the development of the vertex detector with fine pixel CCD at the ILC

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We are developing the vertex detector with a fine pixel CCD (FPCCD) for the international linear collider (ILC), whose pixel size is 5 x 5 μm^2. ILC physics program impose several design requirements, as high granularity and low occupancy. FPCCD also impose several requirements in the readout ASIC, mainly, fast readout speed, low noise and low power consumption as well. We present the status of the R&D in order to achieve those design requirements.

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1. Introduction

One of the most important physics that the ILC is aiming to study is the verification of the Higgs mechanism, which is reflected in the Higgs boson couplings. The measurement of these various couplings requires accurate particle identification; the most crucial one is the separation between b-quarks and c-quarks. In order to realize ILC's highly efficient flavor tagging, we need a vertex detector with an impact parameter resolution of $5 \oplus 10/(p\beta sin^{3/2}(\theta))$ (μm) and a low level of pixel occupancy for accurate track reconstruction. To achieve these two factors the FPCCD uses a finely segmented pixel with the size of 5x5 μm^2 and reads out during the inter-train time 200 ms [1], [2]. FPCCD has several advantages over other proposed options. The finely segmented pixel makes it possible to achieve an impact parameter resolution well below the required 5 μm, i.e. below 1.4 μm. The intertrain readout frees us from beam induced RF noise. The 50 μm thick fully depleted sensor indicates small multiple coulomb scattering and high two track separation capability. Here we will address the performance study results of the readout ASIC for FPCCD vertex detector and its future prospects.

2. FPCCD Detector

Baseline Design Vertex Detector

In order to reach such a high performance level, the ILD vertex detector should comply with the following specifications:

- A spatial resolution near the IP better than 3 μm
- A material budget below 0.15% X_0 /layer
- A first layer located at a radius of $\approx$ 1.6 cm
- A pixel occupancy not exceeding a few %

The power consumption should be low enough to minimise the material budget of the cooling system inside the detector sensitive volume.

Simulations show that such resolution level is feasible with the proposed technologies (Fig. 1).

The baseline design of the ILD vertex detector consists of three, nearly cylindrical, concentric layers of double-sided ladders. Each ladder is equipped with pixel sensors on both sides, $\approx$ 2 mm apart, resulting in six measured impact positions for each charged particle crossing the detector (Fig. 2). The radii covered by the detector range from 16 mm to 60 mm. The material budget of each ladder amounts to $\approx$ 0.3 % X_0, equivalent to 0.15% X_0/layer.

This geometry is independent of the actual pixel technology being finally adopted.

FPCCD

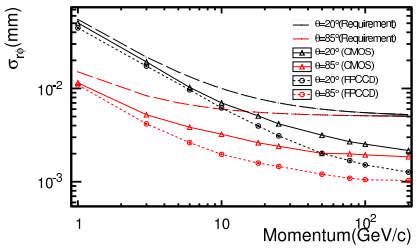

Figure 1: Impact parameter resolution of the ILD vertex detector for two different particle production angles (20° and 85°), assuming the baseline point resolution for the CMOS option (solid line), and the FPCCD option (dotted line). The curves with long dashes show the performance goal.

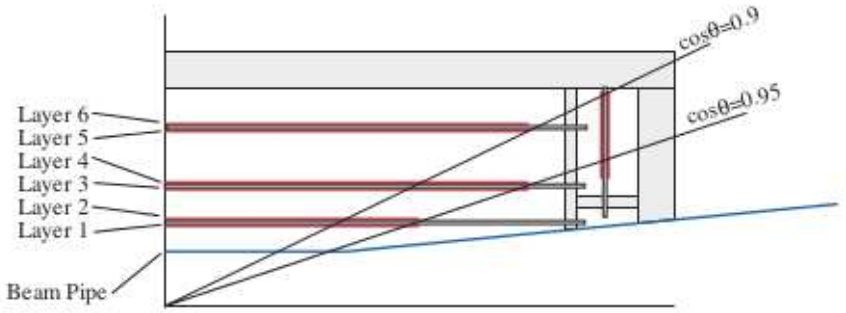

Figure 2: Schematic view of the ILD vertex detector.

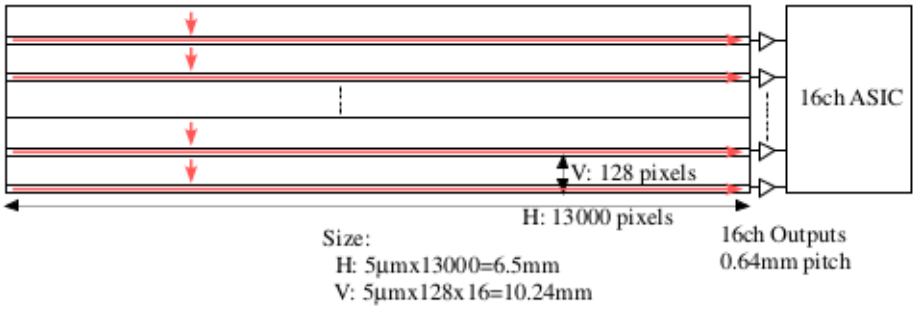

Figure 3: Schematic view of a ladder.

The FPCCD concept is based on the following:

1. Very small pixel size ($\approx 5\ \mu$m).
2. Fully depleted sensitive volume with 15 μm epitaxial layer thickness.
3. Readout between consecutive inter bunch trains.

The first item provide FPCCD detector with excellent two-track separation, and it also reduce the occupancy by beam-related backgrounds. This is particularly important for the inner layers, where those backgrounds at 1 TeV are expected to be very important.

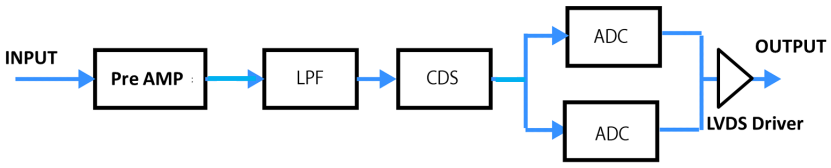

Figure 4: readout ASIC overall architecture

The second item imply the charge spread between neighbourd pixels is very small; this fact has also impact on the two track separation and reduce furthermore the number of hit pixels.

Third item means very fast electronics are not needed, which help to save power consumption. Readout in the inter train has the additional advantage that the FPCCD is intrinsically free of beam-induced RF noise.

Another advantage of using FPCCD, and an unique feature of this sensor technology, it is the use of the cluster shapes to supress the beam-induced backgrounds [3].

CCD is a sort of stablished technology. CCDs have been used for the vertex detector of SLD detector at the Stanford Linear Collider (SLC) and worked excellently [4]. CCDs with the pixel size smaller than 5 μm are widely used for cameras of mobile telephones. FPCCD, therefore, seems a cost-effective technology for future vertex detectors.

Schematic design of the FPCCD sensor is shown in Figure 3. The pixel size is 5 μm square and the thickness of the sensitive layer is 15-20 μm. For the outer layers, the pixel size could be somewhat larger. Each CCD wafer has 16 outputs covering 16 regions, and each region has 128(V) x 13000(H) pixels. The reason why the number of vertical(V) transfer is much less than the number of horizontal(H) transfer is that this configureation is more advantageous for the radiation tolerance. Each region has a horizontal register to transfer the signal charge to the output node. Pixels in the horizontal registers should be sensitive to the charged particles, as well as standard pixels. The frequency to read out the whole pixels in 200 ms with this configuration is $\approx$ 10 Mpixels/s.

The output signals from one edge of the CCD wafer are processed by an ASIC located next to the CCD wafer. This ASIC will have functions of amplifier, low-pass filter, correlated double sampler, and analog-to-digital converter (ADC) for 16 channels (Fig. 4).

3. Status R&D on FPCCD

Small Prototype Tests

We have made small prototype sensors with 6 μm pixel size and full size prototypes for the inner layers (Fig. 5). The readout system has been developed with 3 front-end ASIC'S prototypes already fabricated. The last ASIC prototype matches most of the design requirements [5] when operating at frequences lower than 50 MHz. At high frequecy (100 MHz) it is observed one drop in

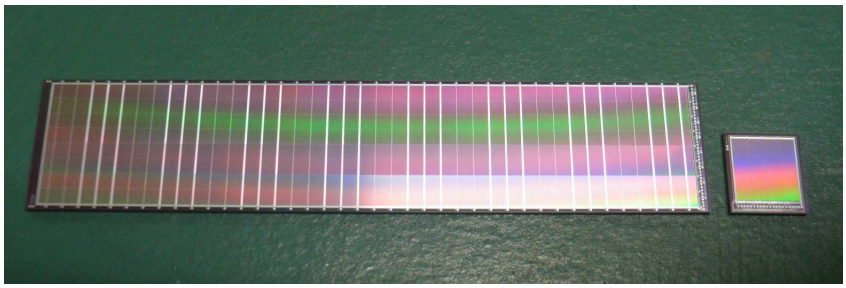

Figure 5: Small and full size prototype sensor with 6 μm pixel size.

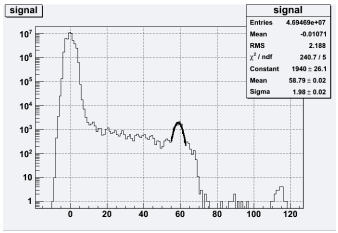

Figure 6: Fe55 peak.

the gain causing one increase in the noise of the readout system. Efforts are foccus in that direction in order to operate the readout system at high frequency with noise levels inside the design limits. Figure 6 shows the sensor response when irradiated with Fe^{55} . The signal peak is visible around 59 ADC.

Recently, we have performed one beam test in order to study the radiation hardness of the sensors. Several CCD were irradiated with a neutron beam. The analysis of these data is ongoing. The estimated neutron flux was $9.4x10^8$ neutron $/cm^2$; the estimated neutron fluence for the inner layers of the ILD vertex detector is $\approx 1.9x10^9$ neutron$/cm^2/year$. We plan to perform a new beam test with higher neutron flux within next fiscal year.

Software R&D

We have developed a new vertex tracking, FPCCD Track Finder [6]. The new track finder keep tracking efficiency high ($\approx 99\%$) until $P_T > 0.6$ GeV. Figure 7 shows the improve in the tracking efficiency for low P_T tracks when using FPCCD with respect to the DBD vertex tracking.

FPCCD Track Finder perform successfully when pair backgrounds are included with minor impact on the tracking efficiency.

FPCCD Track Finder also improve flavour tagging performance compared with previous vertex tracking.

We have found that using a bigger pixel size (10 μm) in the outer layers saves ≈ 30 % power consumption with no mayor impact on the performance [6].

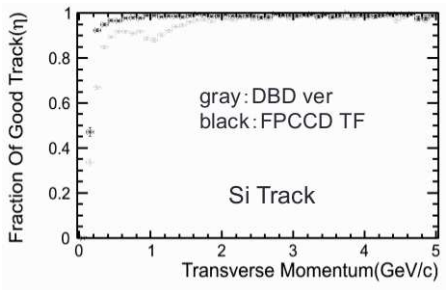

Figure 7: Comparison FPCCD Track Finder with DBD tracking efficiency.

4. Conclusion

Fine pixel CCD (FPCCD) sensors is one of the three sensor technologies being actively developed for the ILD vertex detector. We have cover the status of the R&D in the FPCCD detector. The tests carried out on the small prototypes match the design requirements on noise level and power consumption at low frequency (< 50 MHz).

We have developed a new Silicon Tracking, FPCCD Track Finder, which improves tracking efficiency on low P_T tracks. The new track finder perform well when pair backgrounds are included. FPCCD Track Finder improves the flavour tagging.

We have found that using pixel sizes of 10 μm^2 in the outer layers reduces 30% the power consumption while keeping similar d_0 resolution and occupancy.

Recently we have performed a beam test and analysis on the radiation hardness of the sensors are ongoing. Analysis on Charge Transfer Inefficiency (CTI) for the FPCCD is also under preparation. We plan to perform a new beam test with higher neutron flux during next fiscal year.

References

[1] Y. Sugimoto, et al., *CCD-based vertex detector for GLC*, *Nucl. Instrum. Meth.* **A549** , 87-92, 2005.

[2] Y. Sugimoto, *Fine Pixel CCD Option for the ILC Vertex Detector*, Proceedings of *International Linear Collider Workshop*, Stanford, California, 18-22 Mar. 2005, 550-554.

[3] Y. Sugimoto, et al., *FPCCD Vertex Detector R&D* for ILC, [arXiv:1202.5832 [physics.ins-det]

[4] K. Abe, et al., *Nucl. Instrum. and Meth.* **A400** (1997) 287.

[5] *Development of Readout ASIC for FPCCD Vertex Detector at the ILC*, *IEEE NSS/MIC*, Anaheim, California, October 29-November 3 2012.

[6] *Performance Evaluation and Software Development of FPCCD Vertex Detector in ILC*, *ECFA LC2013*.