# Progress in the development of the vertex detector with fine pixel CCD at the ILC

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Vertex 2013

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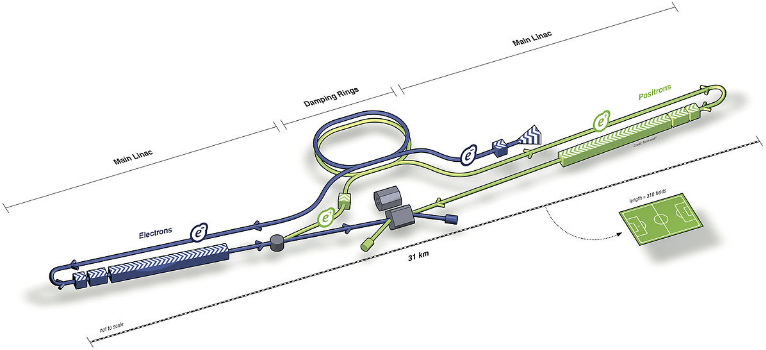
# Outline

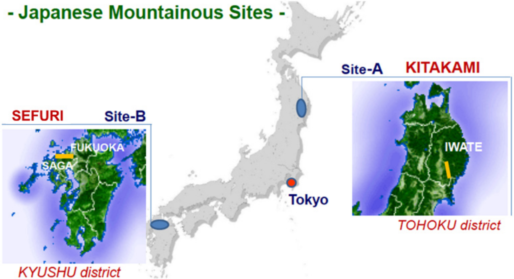
# Introduction

# *Internactional Linear Collider* **ILC**




- $e^+e^-$ linear collider @ 250, 500, 1000 GeV .
- $\approx$ 31 km (50 km after upgrade to 1000 GeV ).
- Beam polarisation ($e^+$,$e^-$)=(20%,-80%)
- L$= 10^{34} cm^{-2} s^{-1}$

# ILC

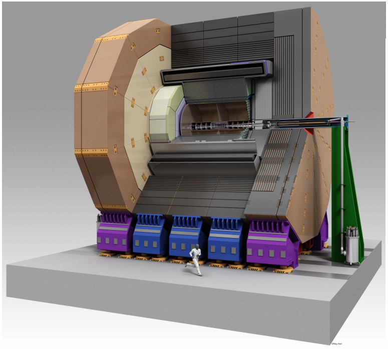


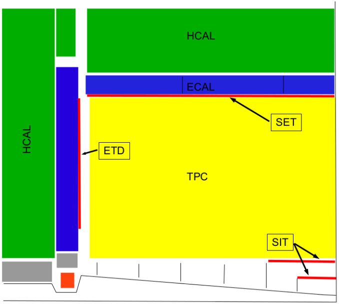

## ILC: important staeps

- Last June *Technical Design Report* (TDR) was published (*).
  - It summarizes many years of global R&D.
- Last month, final selection of the site announced (site-A).

(*)http://www.linearcollider.org/ILC/Publications/Technical-Design-Report

# *Internatinal Linear detector*, **ILD**





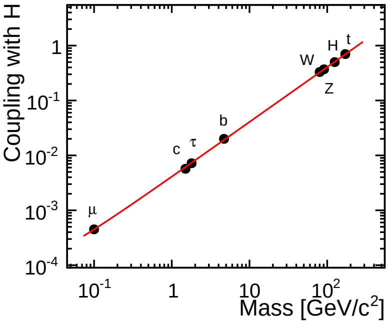

## Multi-purpose detector

- Solenoid $\mathrm{B} = 3.5$ Tesla.
- Pixel vertex detector.
- Time projection chamber.
- Highly segmented electromagnetic (hadronic) calorimeter ECAL (HCAL).

# Importance of the Vertex Detector

## measure Higgs coupling constants

- One of the main topics within the ILC pyisics program.
- To distinguish $\mathrm{H}\rightarrow \mathrm{bb}$ , $\mathrm{H}\rightarrow \mathrm{cc}$ , $\mathrm{H}\rightarrow \mathrm{gg}$ :
  - Precise particle identification.
  - Good separation between b/c quarks.




→ We need a Vertex detector with high performance.

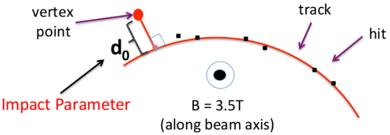
# Physics Requirements on the Vertex Detector

## Impact Parameter Resolution

- Higgs couplings measurements
  $\rightarrow$ Precise particle identification.
  $\rightarrow$ Good separation between b/c quarks.
- Physics goals require vertex detector with impact parameter resolution:

$$d_0 < 5 \oplus 10/(psin^{3/2}(\theta))(\mu\mathrm{m})$$

$\longrightarrow$ FPCCD is designed to provide such resolution.



# Vertex Detector Design

## Design Requirements

- To match $d_0 < 5 \oplus 10/(psin^{3/2}(\theta))(\mu\mathrm{m})$

1. A spatial resolution near the IP better than 3 $\mu\mathrm{m}$
2. A material budget below 0.15% $X_0$ /layer
3. A first layer located at a radius of $\approx$ 1.6 cm
4. A pixel occupancy not exceeding a few %

- To minimise material budget of colling system
  $\longrightarrow$ Low power consumption.

- Several technologies under study to satisfy those design requirements (eg. CMOS, FPCCD, DEPFET).
- In this talk we cover the FPCCD concept.

# Vertex Detector Design

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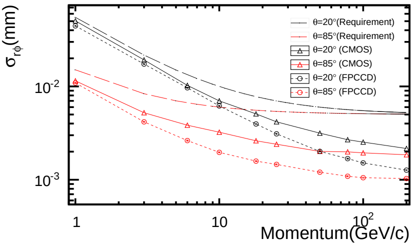



- Simulations show that such resolution level is feasible with the proposed technologies.

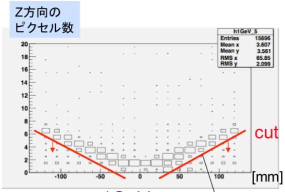
# 2) FPCCD

FPCCD

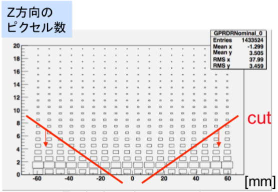
# Fine Pixel CCD (FPCCD)

## Concept

- FPCCD sensors allows small pixel ($\approx 5\ \mu\mathrm{m}$).
  $\longrightarrow$ Provide excellent two-track separation.
  $\longrightarrow$ Reduce the occupancy by beam-related background
  (crucial when integrating signal over many bunch-crossings).
- Sensitive volume is a fully depleted $15\ \mu\mathrm{m}$ thick epitaxial layer.
  Negligible charge spread (Excellent two-track separation, reduce number of hit pixels).
- Readout between consecutive bunch trains (200 ms).
  $\longrightarrow$ No very fast electronics needed.
  $\longrightarrow$ Free of intense beam-induced RF noise.
- Background rejection based on the cluster shapes.
  $\longrightarrow$ Keep low occupancy for inner layers.



1GeV e-

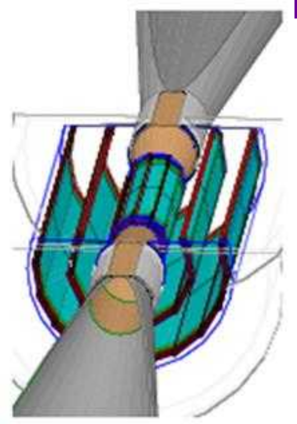


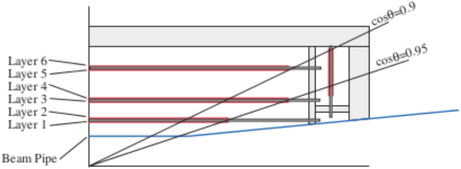
Pair-background

# FPCCD Vertex Detector

## Fine Pixel CCD Vertex Detector

| | $R$ (mm) | $|z|$ (mm) | $|\cos\theta|$ |
|---|---|---|---|
| Layer 1 | 16 | 62.5 | 0.97 |
| Layer 2 | 18 | 62.5 | 0.96 |
| Layer 3 | 37 | 125 | 0.96 |
| Layer 4 | 39 | 125 | 0.95 |
| Layer 5 | 58 | 125 | 0.91 |
| Layer 6 | 60 | 125 | 0.9 |



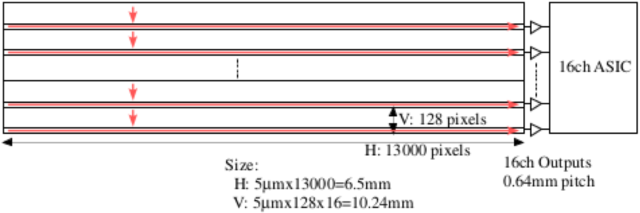



- Inner 2 layers have pixel size 5 $\mu$m and half long.
- External layers may have larger pixels.

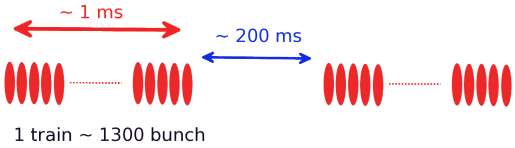
# FPCCD Ladder

## Schematic view innner lader

- 16 channels output.
  → 128*13000 pixels per channel.
- Active circuits localized only on one edge of the wafers.
  → Easy temperature control.



# FPCCD Readout Requirements

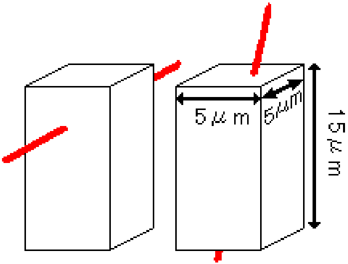



### Readout in the inter train

- Free from RF beam induced noise.
- 13000 $\times$ 128 pixel/ch / 200 ms
  $\rightarrow \approx 10M$pix/sec

### Noise Level $S/N > 10$

- Faint signal level: $\approx$ 500 $e^-$.
- Target noise level w/ CCD: $<$ 50 $e^-$.




### Power consumption

- Required: $< 16\ \mathrm{mW/ch}$ ( $\approx 10\ \mathrm{nW/pixel}$ ):
  - $< 6\ \mathrm{mW/ch}$ (ASIC),
  - $< 10\ \mathrm{mW/ch}$ (CCD).

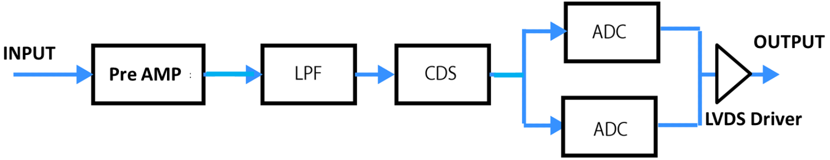
### Cooling

- FPCCD at $-40\ ^\circ\mathrm{C}$ optimal to reduce radiation damage.
- More than 30 $\mathrm{Watt}$ consumed inside cryostat.
- Two-phase $CO_2$ cooling will be used (OD $\sim$ 2 mm cooling tube, 0.3% $X_0$)

# Overal ASIC design

## ASIC elements

- Voltage amplifier.
- Noise: LPF (low pass filter) and CDS (correlated double sampling).
- Readout speed: Two 5 Mpixel/s ADC in parallel.
- LVDS driver.

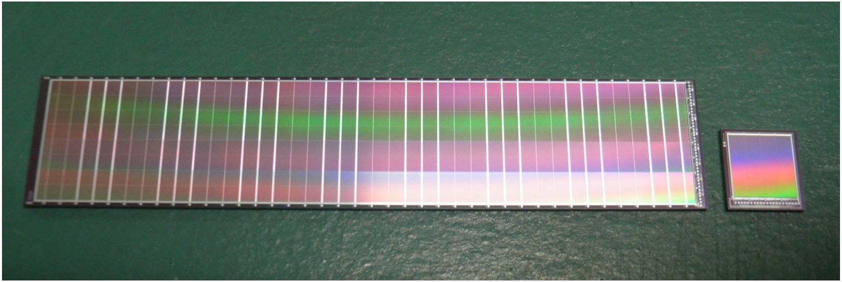


# Status R&D FPCCD

# Status of the R&D I

## Hardware

- Prototype sensors with 6$\mu\mathrm{m}$ size pixel made.
- Full size prototypes for inner layers also made.
- Front-end ASIC's prototypes have been fabricated (3).
- Last ASIC prototype (AFFROC01) shows major improvements in readout speed, differential non linearity(DNL) and power consumption (4.8 $\mathrm{mW/ch}$ ) compared with previous ones.
- Readout system shows good performance at low frequency (25-50 MHz)
  - Getting high gain at 100 MHz is currently under study.



# Status of the R&D II

## Software

- Studying performance of the FPCCD.
  - Optimization of pixel sizes for outer layers.
- Development of a new Silicon Tracking.
  - Better background rejection.
  - Higher efficiency at low $p_T$ .

## Engineering

- Circularing two-phase $\mathrm{CO_2}$ cooling ($-40\ ^\circ\mathrm{C}$) system prototype.

# R&D Our Next Steps

## Performance study

- Demostrate basic performance.
- Spacial resolution.
- Two-track separation.
- Radiation hardness.

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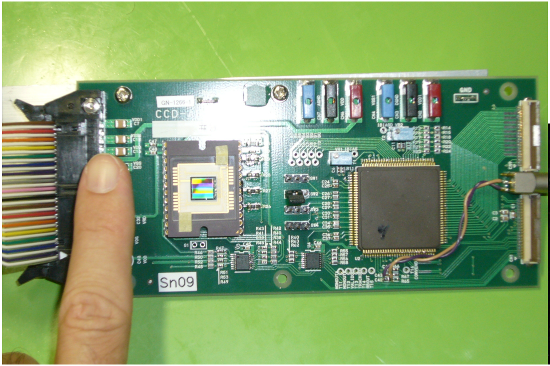
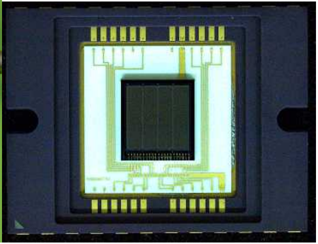
- Reduction of dead space along the edges.
- Test smaller pixel sizes (5 $\mu$m).
- Prototype ladder.
  - 2mm thick, double sided.
  - Material budget $\approx$ 0.3% $X_0$.
  - Mechanical prototype: support shell, endplate, cooling tube, cryostat.

# Small Prototype Tests

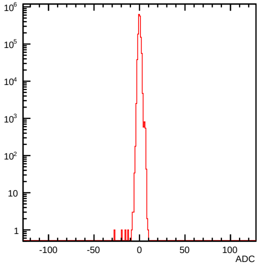
- We are testing the latest readout ASIC (AFFROC01).
- This ASIC prototype has shown major improvements in readout speed, DNL and power consumption.



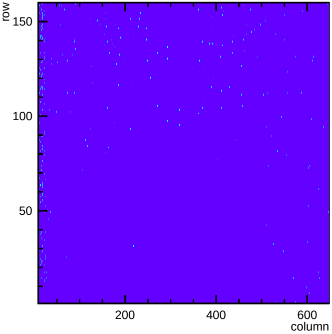



# $^{90}\mathrm{Sr}$ (Preliminary)

- Sensor response to $^{90}\mathrm{Sr}$ radiation (normal incidence).
- Pixel size 9.6 $\mu\mathrm{m}$ , T $\approx$ 25$^{\circ}\mathrm{C}$.
- 2-D plot shows hit pixels.



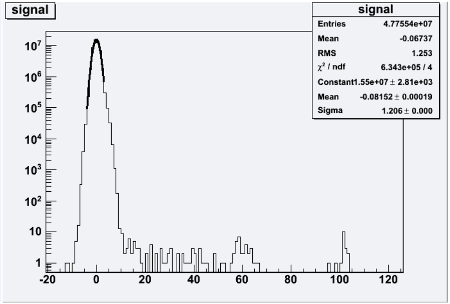

- Pedestal signal.

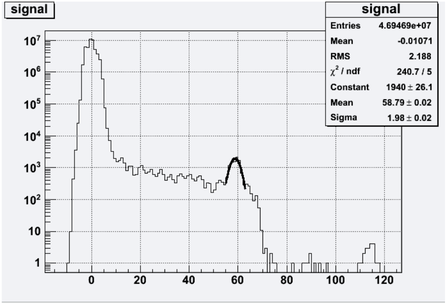



- After $^{90}\mathrm{Sr}$ irradiation.

# $^{55}$Fe Signal (Preliminary)

- $^{55}$Fe signal $\rightarrow$ peak around 60 (right plot).




- Before $^{55}$Fe irradiation.
- After $^{55}$Fe irradiation.

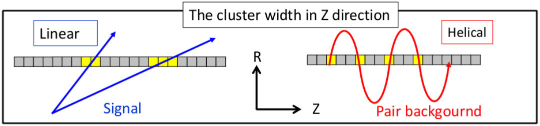
# Software R&D

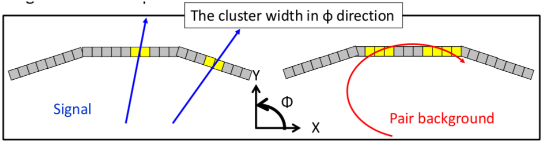
## Aims

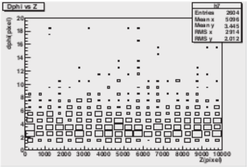
- Improve background rejection at 1 TeV .
- Keep high tracking efficiency at low $p_T$ .
- Optimisation of pixel sizes to reduce power consumption.

# Background Rejection

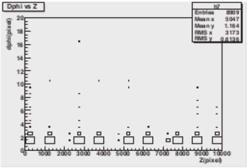
- It is possible exploit the different shape of signal/background clusters.
- Pair back: hit clusters wide in $\phi$, narrow in Z direction.
- High $p_T$ from $e^+e^-$: hit clusters narrow in $\phi$, polar-angle dependent.



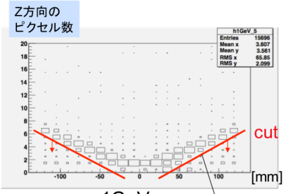



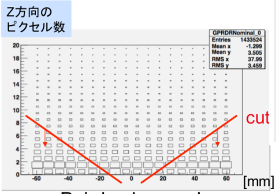




- background $\phi$ distribution.

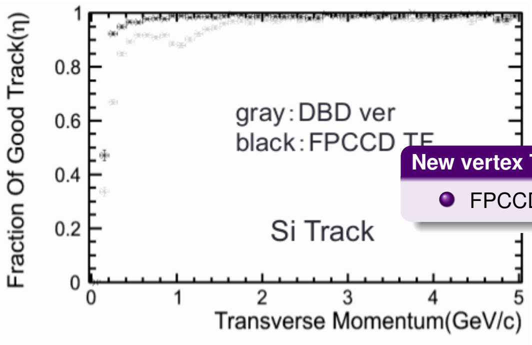



- signal $\phi$ distribution.



# New Vertex Tracking




**New vertex Tracker (FPCCD TF) (*)**

- FPCCD TK improves efficiency for low $p_T$ tracks.

**Optimisation of pixel sizes (*)**

- Configuration using 10 $\mu$m pixel size in outer layers
  - Save 30 % power consumption.
  - Keeps occupancy at 1 TeV $<$ 3 %.
  - Similar IP resolution.

(*)T. Mori *Performance Evaluation and Software Development of FPCCD Vertex Detector in ILC*, ECFA LC2013

# Summary/Outlook

## Hardware: Tests on small prototypes good

- FPCCD satisfying the design requirements.
  - Power consumption (ASIC) 4.8 $\mathrm{mW/ch}$ ($<$6 $\mathrm{mW/ch}$ )
  - Noise level 16 $e^-$ @ 100 MHzCk ($<$ 30)

## Software: Lot of improve here

- Developing a new Silicon Tracking.
  - Efficiency $\approx$ 99 % @ $p_T > 0.6\ \mathrm{GeV/c}$
- Analysis on background rejection by cluster size is ongoing.
- Optimisation of pixel size on outer layers to reduce power consumption.

## Outlook: Still many work to do, stay tune!

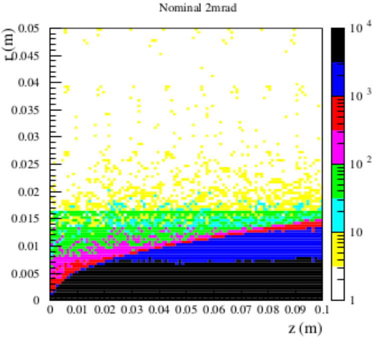
- Radiation tolerance studies.
  - Scheduled neutron beam test this fall.
- Charge transfer inefficiency CTI.
  - CTI Measurement using $^{55}\mathrm{Fe}$ source on preparation.

# Thanks

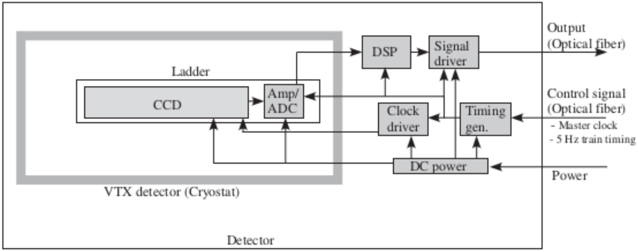
Thank You Very Much!

# Back Up Slides

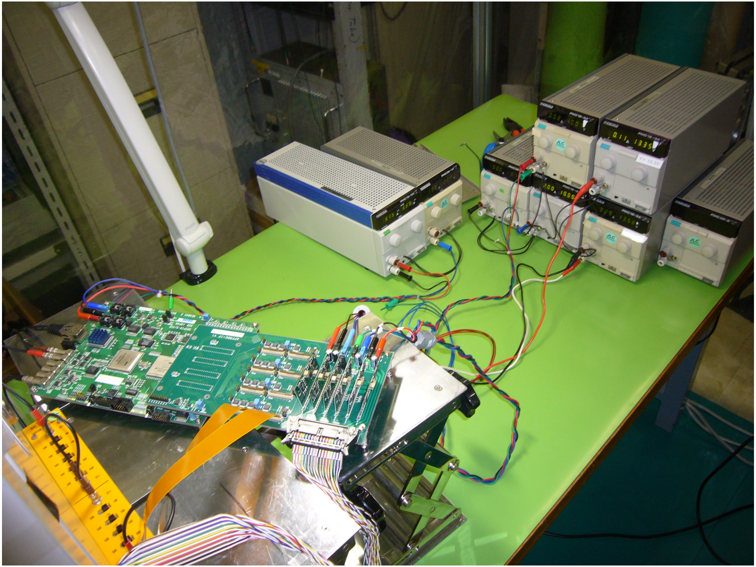
# First Ladder Radium



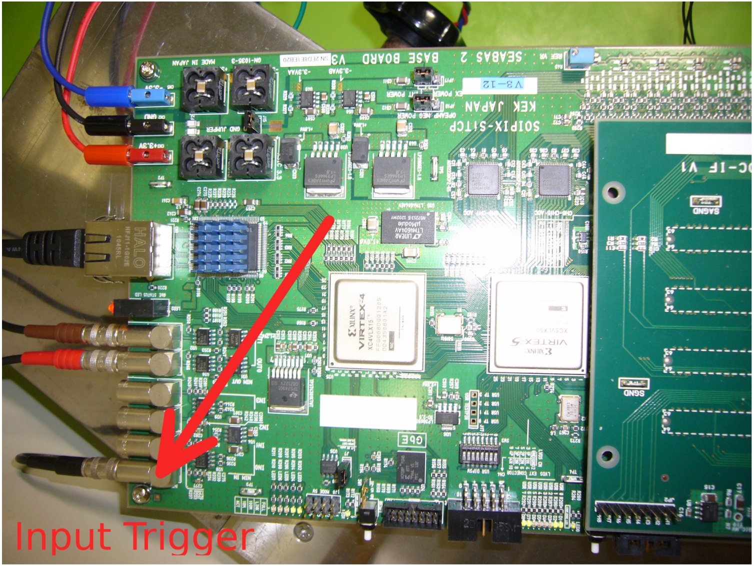
# Readout Schematic



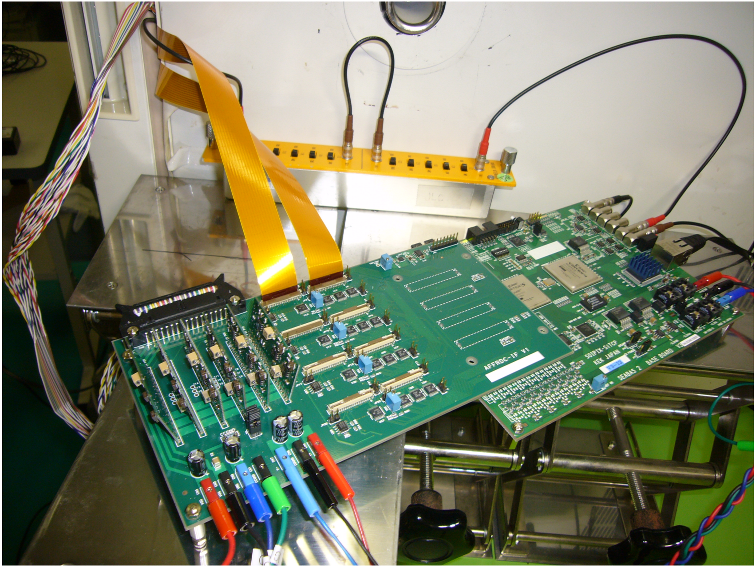
# Test Set Up



# SEABAS 2 Board



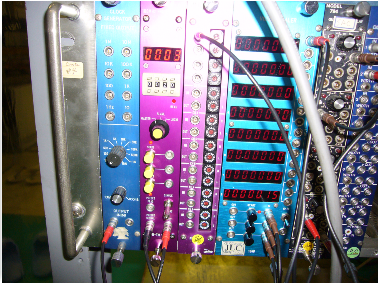
# Affroc & SEABAS2



# External Trigger

## Preselection scaler

- External trigger signal 100 MHz (scaled according with clock signal used)
  $\rightarrow$ In the picture scaled by 20 ($T = 200$ ns) ,for clock signal $T = 40$ ns.

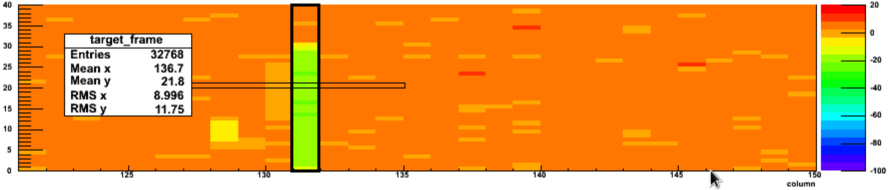


# Humidic Chamber

## Cooling Down

- FPCCD will operate at $-40\ ^{\circ}\mathrm{C}$
  $\rightarrow$ We perform our test as such T.
  $\rightarrow$ Sensor is kept inside this humidic chamber.

- Previous studies shown the fully depleted condition of the sensors.

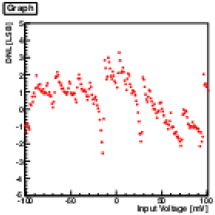


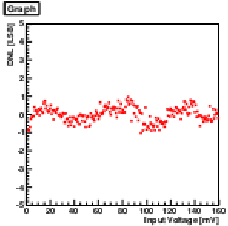

- No charge spread to other pixels observed.

# Improvement on DNL

Differential non linearity (DNL) comparison (100 MHz clock):

- left: FPCCD2B (DNL ±3 LSB)
- right: AFFROC01 (DNL ±0.9 LSB)



# FPCCD2B VS AFFROC01

**Table:** specifications of FPCCD2B and AFFROC01

| chip name | FPCCD2B | AFFROC01 | goals |
|---|---|---|---|
| readout speed | 100 MHz CK | 120 MHz CK | 100 MHz CK (10Mpixels/s) |
| DNL+noise (ENC) | ±3LSB | ±0.9 LSB @ 100 MHZ | |
| noise | 0.97 LSB | 12 $e^-$ ideal gain<br>48 $e^-$ *w*/ observed gain | 30 $e^-$ |
| power consumption | 30.9 mW/ch | 5.8 mW/ch | 6 mW/ch |
| INL | 17 % | $<$ 2 % | N/A |
| baseband transmission | return zero | non-return zero | |