FADC for VTX Readout

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(KEK Online)

On behalf of VTX Group

Outline

- Introduction
- CCD Signal Processor
- New Readout System
  - cPCI-based Readout System
  - New DAQ Platform @KEK
- Summary

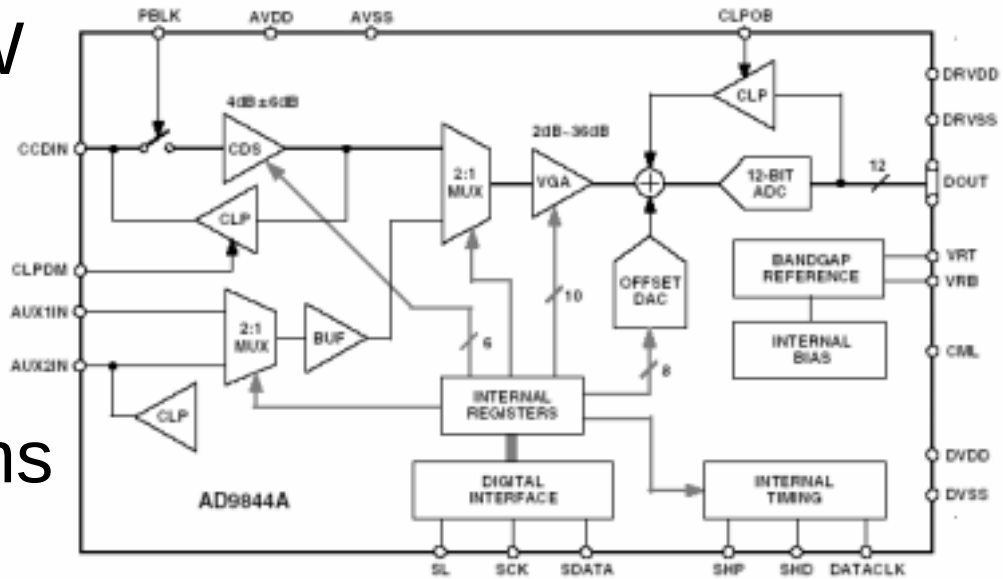
Introduction

- For study of CCD Clock dependence on
  - CTI (Charge Transfer Inefficiency)
  - DCP (Dark Current Pedestal)
  - Hot pixels
- Performance of current readout system is not good enough (2MB/sec).

We need a High-speed (20Mpix/sec) readout system.

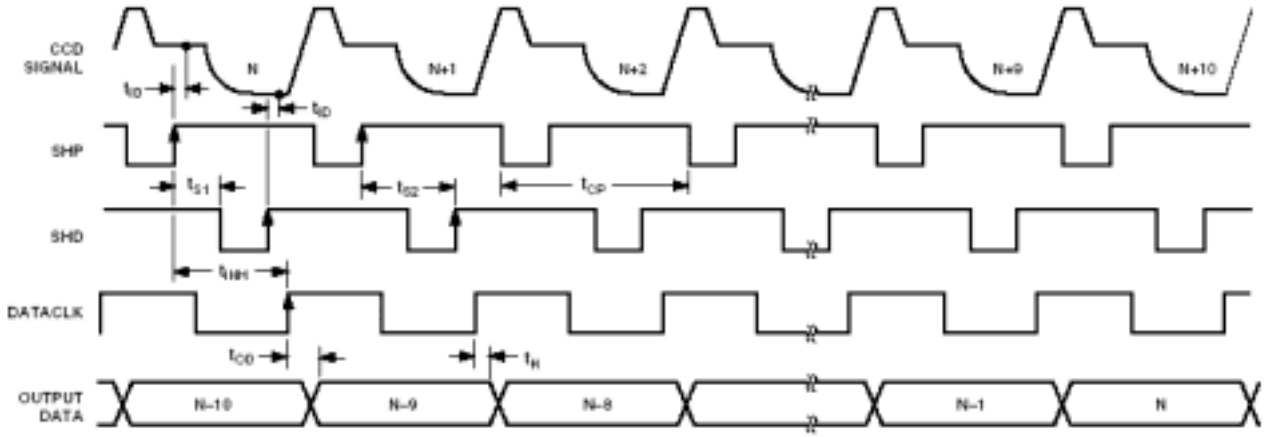
CCD Signal Processor AD9844A

- Features
  - 20MSPS Correlated Double Sampler (CDS)
  - 12Bit 20MSPS A/D Converter
  - 3-Wire Serial Digital Interface
  - Low Power:65mW
  - Low Cost
- Applications
  - Digital Still Cams
  - Digital Video Cams



CCD Signal Processor AD9844A

- Correlated Double Sampler (CDS)

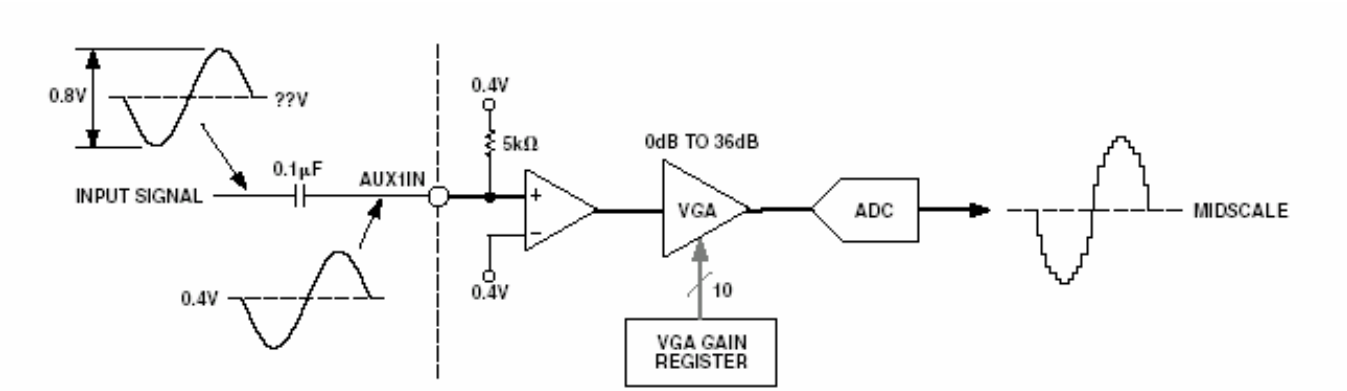


- Internal Register

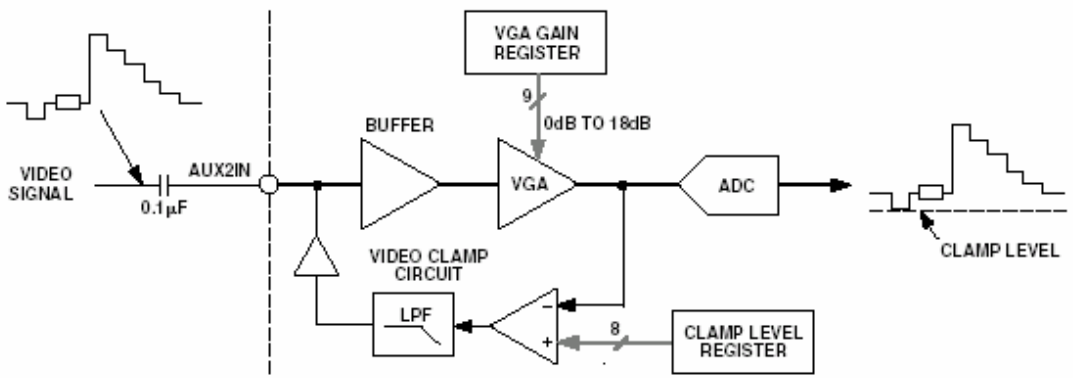
Register Name	Address A0	A1	A2	Data Bits D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
Operation	0	0	0	Channel Select CCD/AUX		Power-Down Modes		Software Reset	OB Clamp On/Off	0*	1**	0*	0*	0*
VGA Gain	1	0	0	LSB									MSB	X
Clamp Level	0	1	0	LSB							MSB	X	X	X
Control	1	1	0	0*	0*	0*	CDS Gain On/Off	Clock Polarity Select for SHP/SHD/CLP/DATA			0*	0*	Three-State	X
CDS Gain	0	0	1	LSB					MSB	X	X	X	X	X

CCD Signal Processor AD9844A

- AUX1 Mode



- AUX2 Mode



cPCI Readout System

- cPCI FADC(AD9844A) Niigata, KEK, RINEI
  - 4ch CCD Input
  - External 3 clocks (LVDS)
  - 1Mwords Memory/ch
- CPU (Sanritz Automation)
  - Pen4-M 2.2GHz
  - ServerWorks GC-LE
  - 1000Base-T 2ch, 100Base-Tx 2ch
- Crate(EBRAIN)
  - 5Slots

Status of cPCI Readout System

- Digital Part test: *Done @KEK*
- Device Driver: *Done @KEK*
- Integrated test: *Resuming @Niigata Univ.*
  - AUX1 mode Test: *Done*

Issues of cPCI FADC

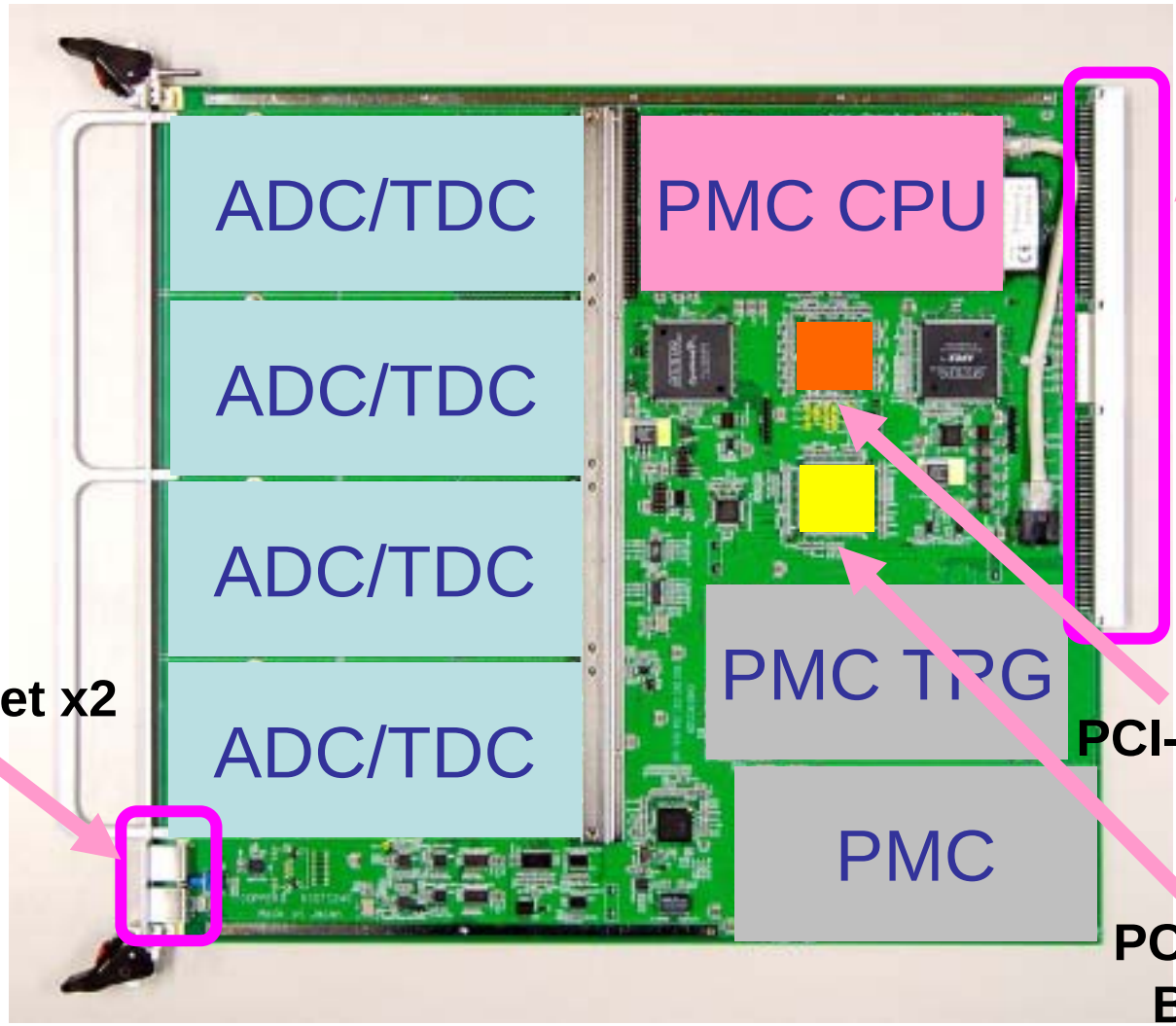
- The current version of FADC can not be operated with DMA transfer mode.
- We have to add DMA transfer logic to it for high-speed readout.
- It will take a good amount of time to complete.

Another Solution?

New DAQ Platform @KEK

- **COPPER** (COmmon Pipelined Platform for Electronics Readout)
  - PCI bus based Mother Board(9U VME)
- **FINESSE** (Front-end INstrumentation Entity for Sub-detector Specific Electronics)
  - Simple designed I/O card
- **PMC Processor** (Pen III 800MHz, Linux 2.4.x)
- **KEK VME Crate 9U**

COPPER



VMEbus

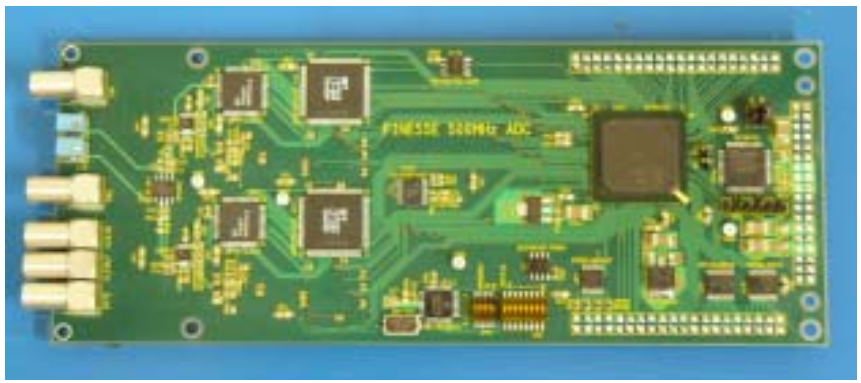
Ethernet x2

PCI-to-LocalBus Bridge

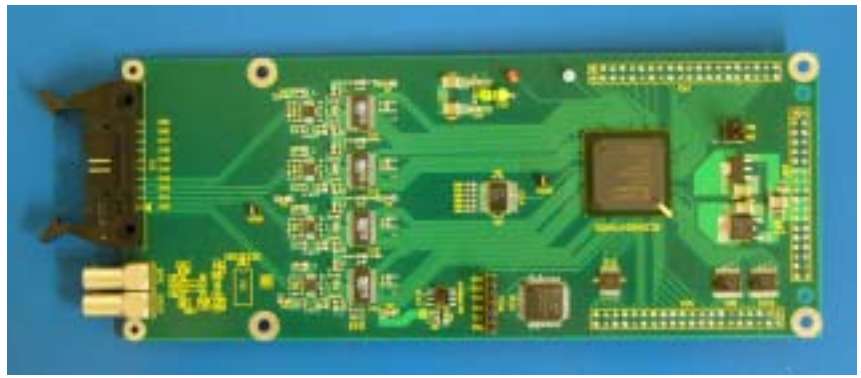
PCI-to-PCI Bridge

FINESSE

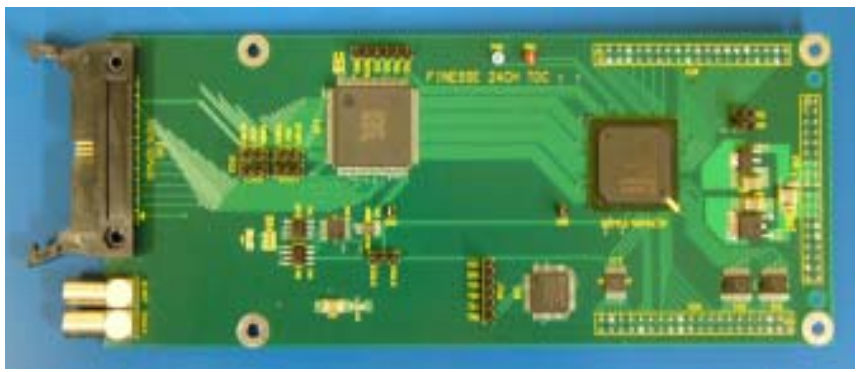
2ch 500MHz FADC



8ch 65MHz FADC



24ch TMC TDC



2ch 20MHz CCD FADC

Developed by K. Tauchi@KEK Elec. Group

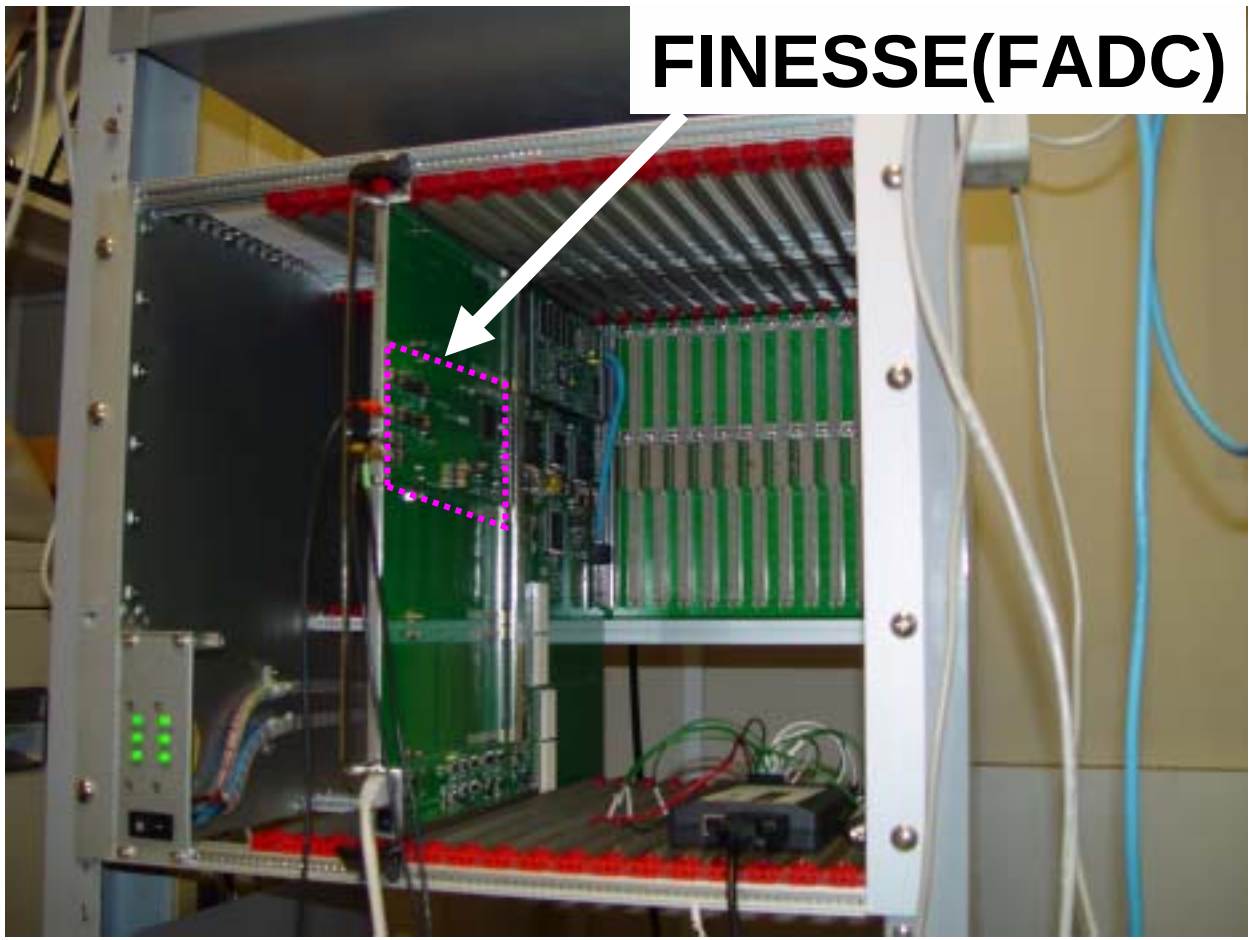
Processor PMC

RadiSys EPC-6315

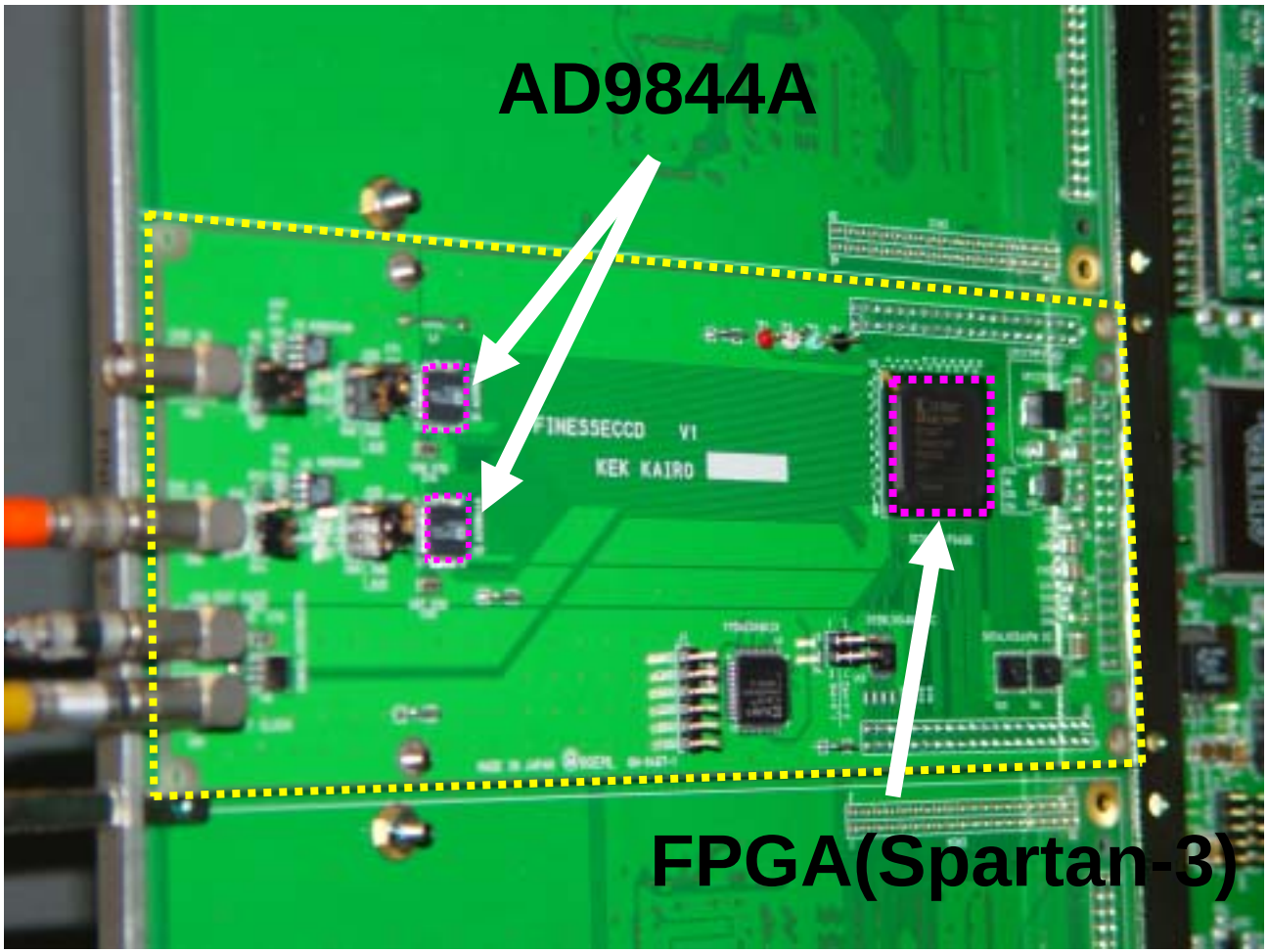
- RadiSys 82600 Chipset
- 800MHz Pentium III-M
- 32bit 66MHz PCI I/F
- 10/100 Base T Ethernet
- CompactFlash

OS: Linux(2.4.x)

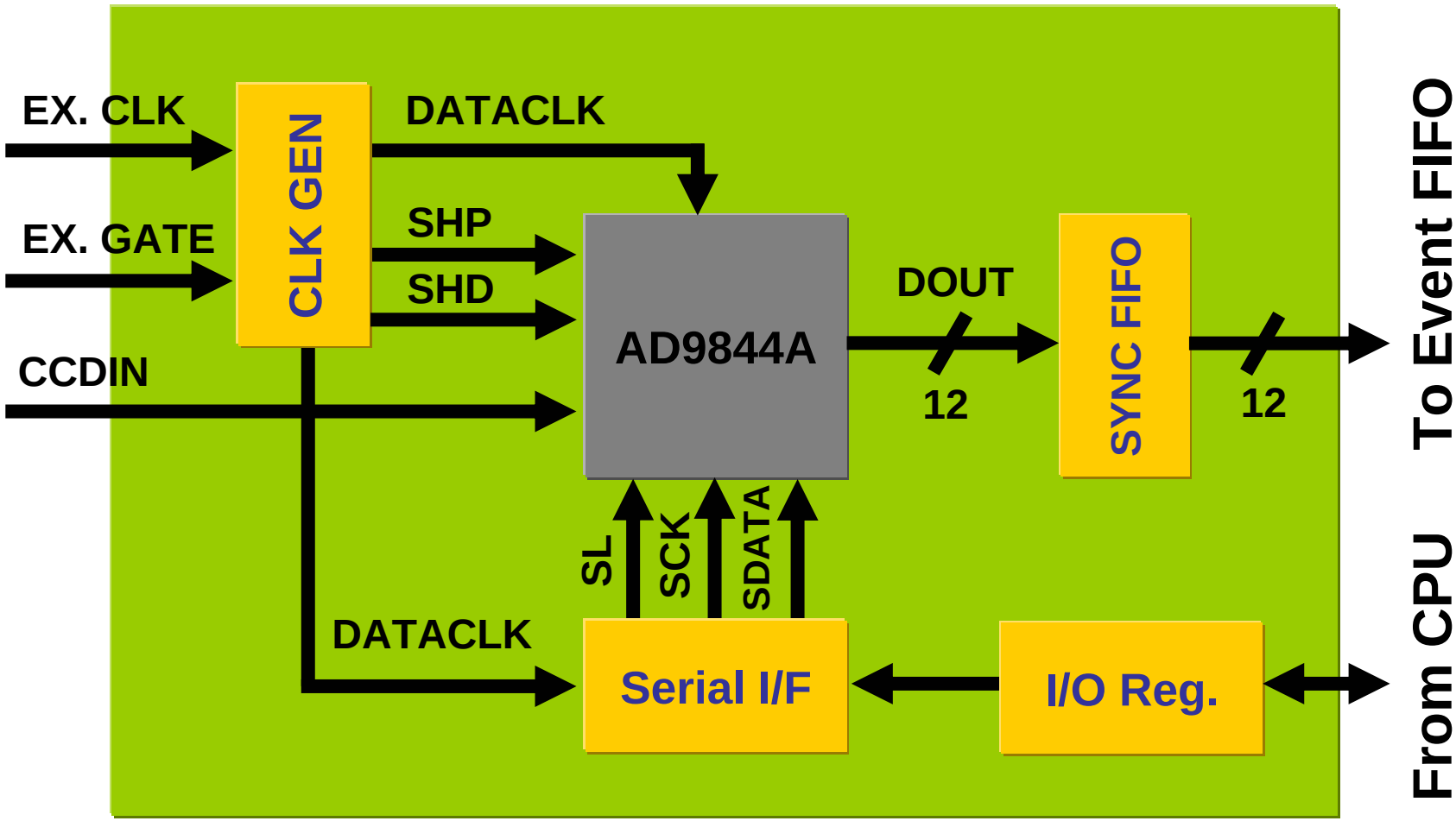
Test Bed



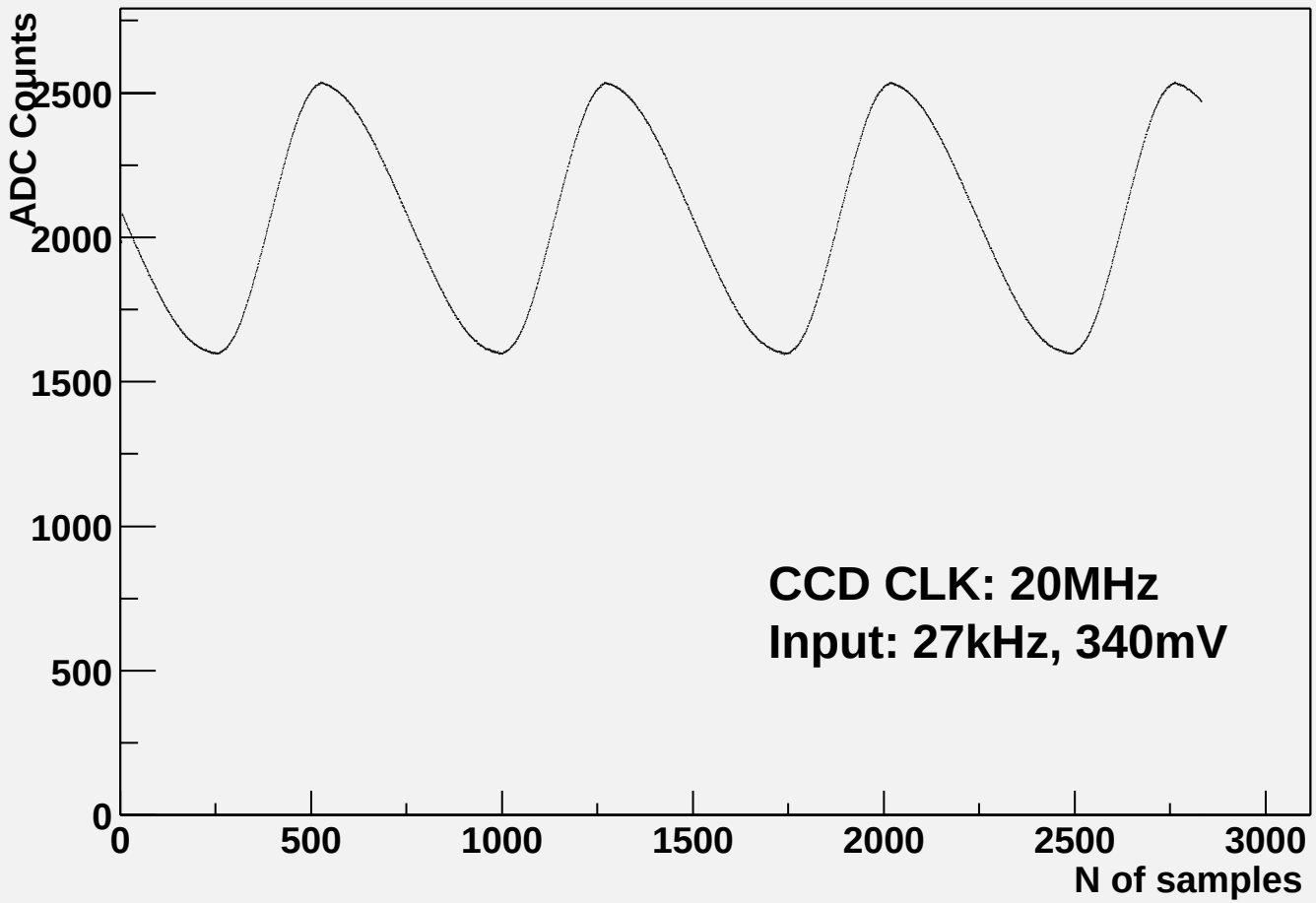
FINESSE CCD-FADC Prototype



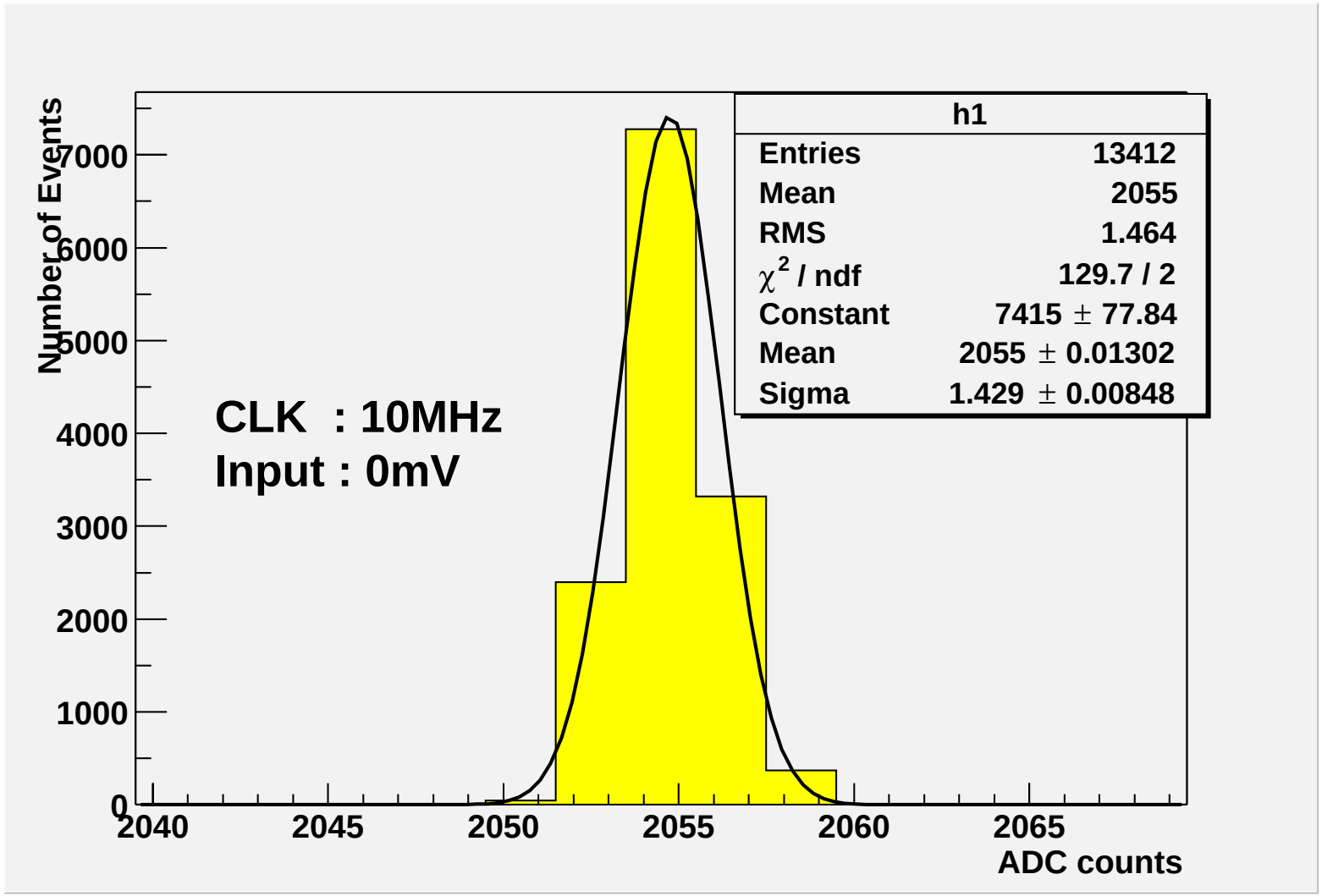
FINESSE CCD-FADC Prototype



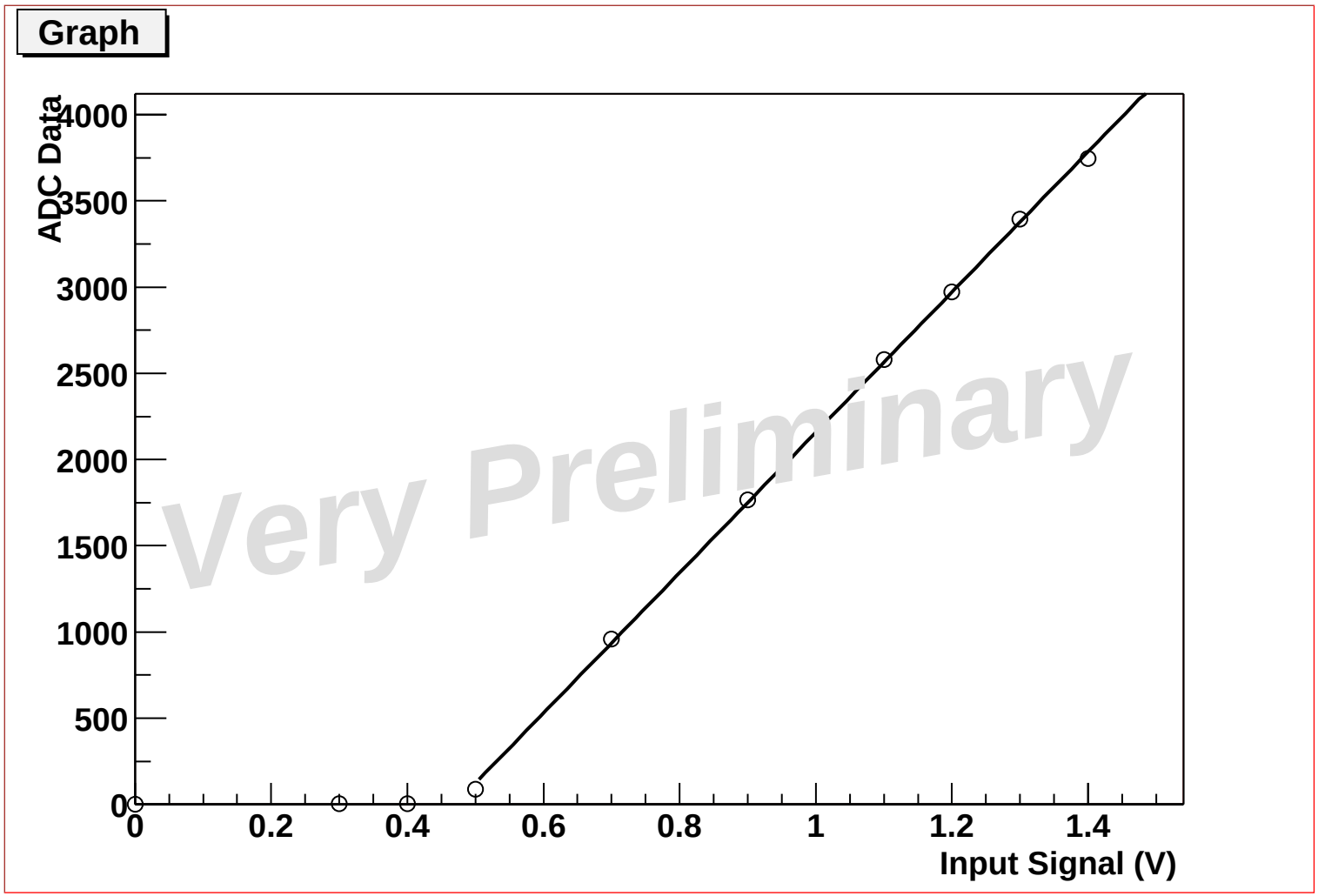
FADC AUX1 Mode Test



FADC AUX1 Mode Test



FADC CCD Mode Test



Status of FINESSE FADC

- Logic Programming: *Almost Done*
  - CCD 3 CLOCKs
  - Serial Interface
  - I/O Register
  - FIFO
- PIO read Test: *Done*
- AUX1 mode Test: *Done*
- CCD mode Test: *Going*

Summary

- We are working to build High Speed Readout System for study of CLK dependence on CTI, DCP, Hot Pixels.
- We have two options;
  - cPCI based Readout system
  - New DAQ Platform
- Now testing FINESSE-FADC Prototype
  - PIO read from COPPER's Event FIFO was checked out
- Resumed cPCI FADC work @Niigata Univ.

Schedule

- Finalize the logic programming of FINESSE FADC
  => By the end of March
- Test using real CCD signals
- High-Speed readout test using DMA transfer on COPPER
  => March - April
- Resume cPCI FADC work @KEK
  => April - May?